國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

具有低輸入電流峰值抽載特性之

正負高壓產生器及其在生醫晶片上之應用

Design of High-Voltage Generator with Low Supply Peak Current for Biomedical Applications

研 究 生: 鄭莞學　　(Wan-Hsueh Cheng)

指導教授: 柯明道教授 (Prof. Ming-Dou Ker)

中華民國一○四年十月

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碩士論文

A Thesis
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October 2015
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摘要

近年來，由於生醫科學與半導體電子的快速發展，電刺激技術已被證明可藉由電流訊號刺激神經來恢復身體的某些功能，例如視網膜、癲癇抑制、電子耳等。在輸出電流刺激時，由於生物組織的阻抗較高，所以在刺激時在組織兩端會有高電壓，故在生醫晶片中需要產生一高電壓與可耐高壓之刺激器。

電荷幫浦(charge pump)依據不同的架構可由低電壓產生正高壓與負高壓，此篇論文提出一正高壓電荷幫浦與一負高壓電荷幫浦，並使用低壓製程製作，使用之電荷幫浦架構沒有閘極可靠度(gate-reliability issue)的問題，量測分別可產生 10.8V 與-10.3V 高電壓，並使用回授控制使輸出電壓穩定，最大可輸出 3.5mA 電流。改變電荷幫浦每級控制訊號，使 3.3V 之最大輸入瞬間抽載變小，且用四個不同相位之控制訊號可減小電荷幫浦之漏電流(return-back leakage current)的影響，

改善電荷幫浦之效率。全電路皆實現在晶片上，不需要外掛電容，適合與其他電路整合在生醫單晶片上，此電路在 TSMC 0.18μm 1.8-V/3.3-V CMOS 製程下實現。

Design of High-Voltage Generator with Low Supply Peak Current for Biomedical Applications

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Abstract

Nowadays, due to the development of biomedical science and electronics, electrical stimulation had been proven can recover some physical functions of patients by current stimulation such as retinal stimulation, cochlear implant and suppression of epileptic seizure. Because the impedance of tissues is large, the voltage between tissues would be high when the stimulator driver deliver stimulus current. Therefore, we need to generate high voltage and high voltage tolerant stimulus drivers.

Charge pump can generate high positive voltage or high negative voltage from low voltage by different charge pump circuit. A positive charge pump and a negative charge pump has been designed to generate high voltage and negative without gate-reliability

issues in low voltage CMOS process. By measurement, the charge pumps can output regulated voltage about 10.8V and maximum current 3.5mA. The output voltage is regulated by PFM control feedback. The maximum output current is 3.5mA. The clock of each charge pump stage has phase shift different from each other, which can reduce the maximum peak current from 3.3V supply. The charge pump also adopt 4-phase clock scheme, which can reduce the return-back leakage and increase the charge pump's efficiency. The charge pump circuit is fully on chip and had been fabricated in TSMC 0.18μm 1.8-V/3.3-V CMOS process.

Contents

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感謝柯明道老師在這兩年的教導，讓我學到了非常多的東西，不僅僅是在專業領域上的精進，更學到了許多做事的態度。此外，也感謝老師讓我參與癲癇計畫及電子耳計畫，可以接觸到一些電子領域外的東西，也要感謝交大眾多教授的指教，每一堂課都對我的研究有很大的助益。

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最後感謝爸我的父母，從小到大給予栽培與經濟支持，讓我能無憂無慮的成長與順利的完成學業。

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Chapter 1
Introduction

1.1 Motivation

As bioelectronics developed, many stimulators have been investigated and demonstrated. For biomedical stimulation circuit, we need to generate a high voltage to drive stimulator and the stimulus chip need to be small for implantation. So, the stimulus circuits are designed fully on-chip. However, the on-chip inductor is about ~nH, which is difficult to be used in boost converter.

Charge pump circuit use capacitors and switches to pump charge and can generate high voltage which is higher than the supply voltage from low voltage. Moreover, charge pump can generate high voltage by high switching frequency with capacitors fully on-chip. So, it is suitable for implantation circuit in low voltage process.

Some problems of conventional charge pump circuit had been studied, such as body effect, gate-reliability issues, threshold voltage drop, and return-back leakage current.

In this work, by adopting 4-pahse charge pump and PFM feedback, we designed a positive charge pump and a negative charge pump can output regulated voltage without the problems of conventional charge pump circuit. Moreover, we apply phase shift clock control scheme. The control clock of each charge pump stage has phase shift different from each other, which can decrease the peak input current from supply and can enhance the transient response of the front dc-dc converter.

1.2 Thesis Organization

This thesis is organized into five chapters and this introduction is the first one. Chapter 2 introduces the applications and the prior arts of charge pump circuits. In chapter 3, a charge pump circuit which can generate 11V is presented, and the measurement results are also shown in this chapter. In chapter 4, a new cross-couple negative charge pump circuit without the gate-oxide reliability issues and reducing the return-back leakage current is presented, and the measurement results are also shown in this chapter. Chapter 5 is the conclusions of this thesis and the future works of charge pump circuits.

Chapter 2

Prior Arts of Charge pump Circuits

2.1 Applications of Charge Pump Circuits for Biomedical Implants

Nowadays, biphasic stimulators are generally used for retinal, cochlear, and neural [1]~[3]. The biphasic stimulators can output anodic and cathodic stimulus current. Because tissue has high impedance, the supply voltage of stimulators need to be high. Some biphasic stimulators use both high positive voltage and high negative voltage for stimulus drivers [1]. For biomedical implants, the area of implanted chip should be small and the use of off-chip elements should be decreased, so CMOS technologies are suitable to realize the system on a chip (SoC). Therefore, the charge pump circuits should be realized in low-voltage CMOS processes and better be fully on-chip. Fig.2.1 depicts the architecture of epileptic stimulation SoC. It use wireless power to supply the implant part. The high voltage generator is integrated with other circuits in single chip.

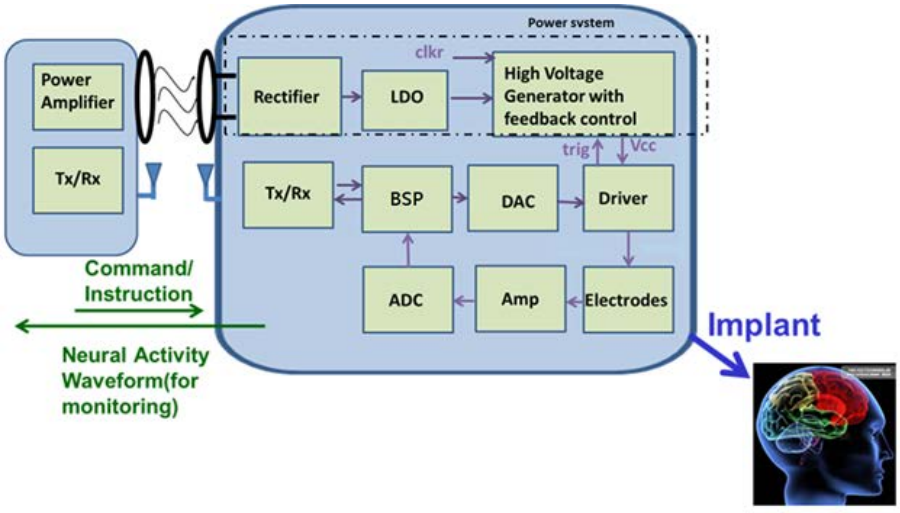


Fig. 2.1 Architecture of epileptic stimulation SoC.

2.2 Positive Charge Pump Circuit

2.2.1 Dickson Charge Pump

Fig. 2.2 depicts the Dickson charge pump [4], which consists of diodes and pumping capacitor (C). C_P is parasitic capacitor and C_O is output capacitor. When clk is logic high (clkb is logic low), the even stage diodes are turn on, the odd stage diodes are turn off. Also, when clk is logic low (clkb is logic high), the even stage diodes are turn off, the odd stage diodes are turn on. The charge can be delivered from front stage to the next stage. Due to the parasitic capacitor (C_P), the voltage swing of each node is the clock swing (V_{clk}) divided by capacitance divider. Since the total charge pumped by diode during each clock cycle is output loading current (I_{load}) multiply by the clock period (1/f), the voltage drop of each stage can be shown as (2.1). Also, each stage has the diode forward voltage drop (V_D), the voltage fluctuation of each stage can be shown as (2.2). For N stage Dickson charge pump, the output voltage is shown as (2.3).

$$\Delta V_{drop} = \frac{I_{load}}{f(C+C_P)} \tag{2.1}$$

$$\Delta V = V_{clk} \times \frac{C}{C+C_P} - \frac{I_{load}}{f(C+C_P)} - V_D \tag{2.2}$$

$$V_O = N\left(V_{clk} \times \frac{C}{C+C_P} - \frac{I_{load}}{f(C+C_P)} - V_D\right) - V_D \tag{2.3}$$

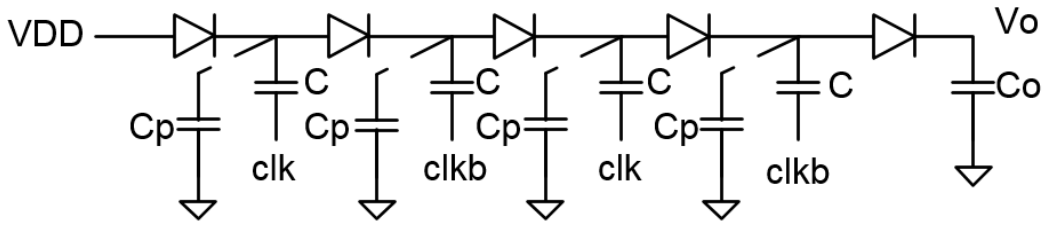


Fig. 2.2 Dickson charge pump with diode.

Fig. 2.3 is the Dickson charge pump with NMOS [5], which consists of diode connected NMOS, pumping capacitor and output capacitor. The same as the conventional charge pump, each stage has the voltage drop of MOS threshold voltage (V_t). In this circuit, if the MOS body don't connect with MOS source, it has body effect,

which may increase conduction loss of MOS switch. Therefore, the efficiency of this circuit is decreased as the stage increases. Besides, the maximum voltage difference between MOS source and drain is $2V_{clk}$-V_t. In low voltage process, the MOS may have gate-reliability issues.

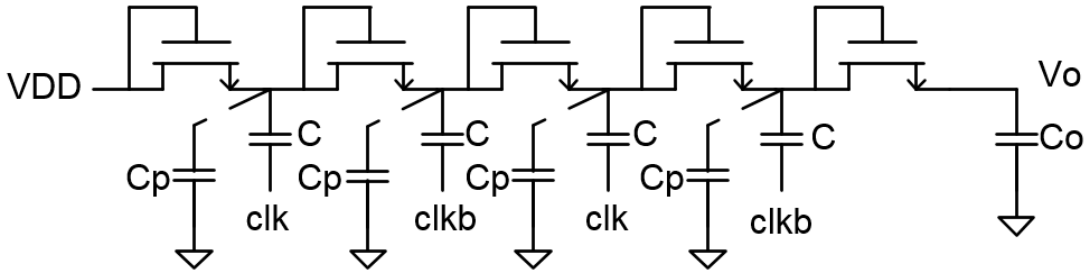


Fig. 2.3 Dickson charge pump with NMOS.

2.2.2 Charge Transfer Switches Charge Pump

Fig. 2.4 depicts the charge transfer switches (CTS's) charge pump [6], which consists of diode connected MOS (MD1~MD6), charge transfer switch (MS1~MS4), pass transistors (MN1~MN4 and MP1~MP4), pumping capacitor (C) and high-voltage (HV) clock generator. The CTS's in this circuit can be turned off completely and each stage doesn't have forward voltage drop and threshold voltage drop as the conventional Dickson charge pump.

When clk is logic low (clkb is logic high), MP1 is turned on and then MS1 is turned on to transfer V_{DD} to node 1 without threshold voltage drop. At the same time, MN2 is turned on to cut off MS2 for reducing leakage from node 2 to node 1. Similarly, when clk is logic high (clkb is logic low), the voltage of node 1 is $2V_{DD}$. MP2 is turned on and then MS2 is turned on to transfer $2V_{DD}$ to node 2 without threshold voltage drop. At the same time, MN1 is turned on to cut off MS1 for reducing leakage from node 1 to V_{DD}.

Following this operation, the voltage can be pumped high with high efficiency, but there is a threshold voltage drop (V_t) at the last stage (MD5). In order to generate control waveform to control MS4, MD6 and C_{HV} are added. Besides, the HV clock generator is added to let MS4 can turn on in low supply voltage operation. The HV clock generator can generate $0\sim2V_{DD}$ clock and the circuit is shown as Fig. 2.5.

This charge pump circuit utilizes charge transfer switches to transfer charge without threshold voltage drop, but it still has the threshold voltage drop at the last stage.

Besides, the maximum voltage difference across MOS is $2V_{DD}$, which cause gate-reliability issues. Due to the parasitic capacitor (C_P) and loading current (I_{load}), the output voltage is shown as (2.4).

$$V_O = N\left(V_{clk} \times \frac{C}{C+C_P} - \frac{I_{load}}{f(C+C_P)}\right) - V_t \tag{2.4}$$

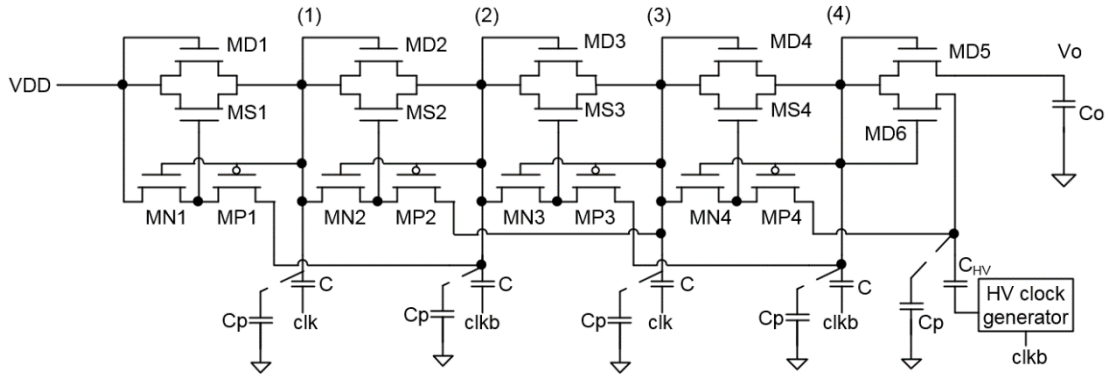


Fig. 2.4 Circuit of charge transfer switches (CTS's) charge pump.

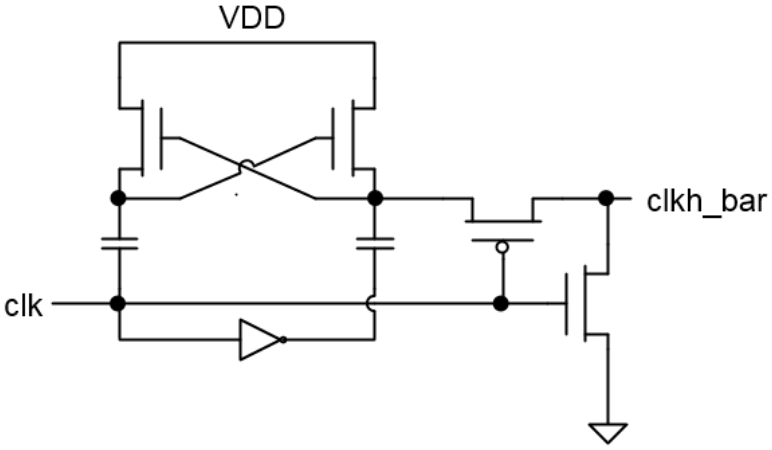


Fig. 2.5 High voltage (HV) clock generator.

2.2.3 Cross-Couple Charge Pump

Some modified charge pump circuits based on Dickson charge pump were invented to overcome threshold voltage drop and to improve pumping gain and efficiency. However, those charge pump circuits have gate-oxide reliability issues because of the gate-source voltages and gate-drain voltages exceed normal operating voltage of MOS. In order to overcome gate-oxide reliability issues, some charge pump circuits were proposed. Fig 2.6 depicts the cross-couple charge pump [7], which was

designed without overstress voltage across MOS and realized in low voltage CMOS process.

When clk is logic low (clkb is logic high), the voltage of node 1 become V_{DD} and the voltage of node 2 become $2V_{DD}$ due to clkb. At the same time, Mn1 is turned on and Mp1 is turned off. Mn2 is turned off and Mp2 is turned on. The voltage of node 4 become $2V_{DD}$.

Similarly, when clk is logic high (clkb is logic low), the voltage of node 2 become V_{DD} and the voltage of node 1 become $2V_{DD}$ due to clk. At the same time, Mn2 is turned on and Mp2 is turned off. Mn1 is turned off and Mp1 is turned on. The voltage of node 3 become $2V_{DD}$. By these operations, the voltage can be pumped high without gate-oxide reliability issues. Moreover, this circuit doesn't have threshold voltage drop by using MOS switches to transfer charge. Besides, this circuit used two branches, which can have less output voltage ripple at the output.

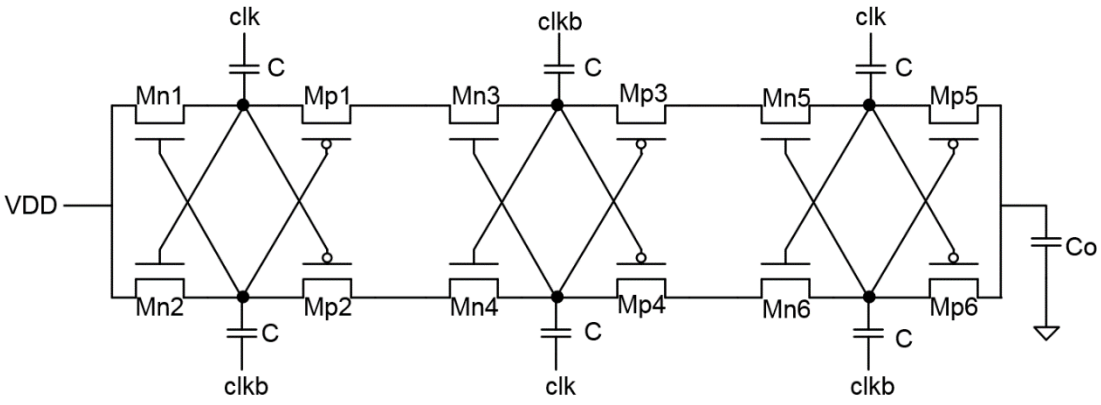


Fig. 2.6 The cross-couple charge pump.

2.3 Negative Charge Pump Circuit

2.3.1 4-phase Negative Charge Pump with PMOS Charge Transfer Switches

Fig.2.7 depicts the negative charge pump [8], which consists of PMOS transfer switches and pumping capacitors. The last stage used diode connected PMOS to prevent

leakage current. This charge pump use 4-phase clock scheme to control PMOS transfer switches, the 4-phase clock is shown as Fig.2.8.

Here, we separate 4-phase clock to eight intervals. At the interval t_1, the voltage of node 1 is GND and the voltage of node 2 is $-V_{DD}$, where V_{DD} is the voltage swing of clock. The voltage of node 3 is $-2V_{DD}$ and the voltage of node 4 is $-V_{DD}$. Mp1 and Mb1 are turned off, and Mb1 and Mp2 are turned on to transfer charge.

At the interval t_2, the voltage of F4 is rose to high (V_{DD}). The voltage of node 3 is rose to $-V_{DD}$ to cut off Mp2. The voltage of node 1, node 2 and node 4 are the same as the voltage at interval t_1. Mp1 and Mp2 keep being turned off and Mb1 keep being turned on.

At the interval t_3, the voltage of F1 is dropped to low (GND). The voltage of node 4 is dropped to $-2V_{DD}$. The voltage of node 1, node 2 and node 3 are the same as the voltage at time interval t_2. Mp2 keep being turned off to prevent leakage current from node 2 to node 4 and Mb2 is turned on by the voltage drop of node 4. Mp1 keep being turned off, and Mb1 keep being turned on.

At the interval t_4, the voltage of F3 is rose to high (V_{DD}). The voltage of node 2 is rose to GND to cut off Mb1 and the voltage of node 3 is charged to GND to keep cut off Mp2. The voltage of node 1 and node 4 are the same as the voltage at time interval t_3. Mp1 keep being turned off and Mb2 keep being turned on to transfer charge from node 2 to node 3.

At the interval t_5, the voltage of F2 is dropped to low (GND). The voltage of node 1 is dropped to $-V_{DD}$ to turn on Mp1 and the voltage of node 2 become GND. The voltage of node 3 and node 4 are the same as the voltage at time interval t_4. Mp2 keep being turned off and Mb2 keep being turned on.

At the interval t_6, the voltage of F2 is rose to high (V_{DD}). The voltage of node 1 is rose to GND to turn off Mp1. The voltage of node2, node 3 and node 4 are the same as

the voltage at time interval t_5. Mp2 and Mb1 keep being turned off and Mb2 keep being turned on.

At the interval t_7, the voltage of F3 is dropped to low (GND). The voltage of node 2 is dropped to $-V_{DD}$ and the voltage of node 3 is dropped to $-V_{DD}$ as well. The voltage of node 1 and node 4 are the same as the voltage at time interval t_6. Mp1, Mb1 and Mp2 keep being turned off and Mb2 keep being turned on.

At the interval t_8, the voltage of F1 is rose to high (V_{DD}). The voltage of node 4 is rose to $-V_{DD}$ to turn off Mb2. The voltage of node1, node 2 and node 3 are the same as the voltage at time interval t_7. Mb1, Mp1 and Mp2 keep being turned off.

By these operations, the voltage of output can pumped to negative high voltage. The advantage of this pump is no leakage current by 4-phase clock scheme. However, the maximum voltage stress on PMOS is as high as 2VDD, which may cause gate-reliability issues in low voltage CMOS process.

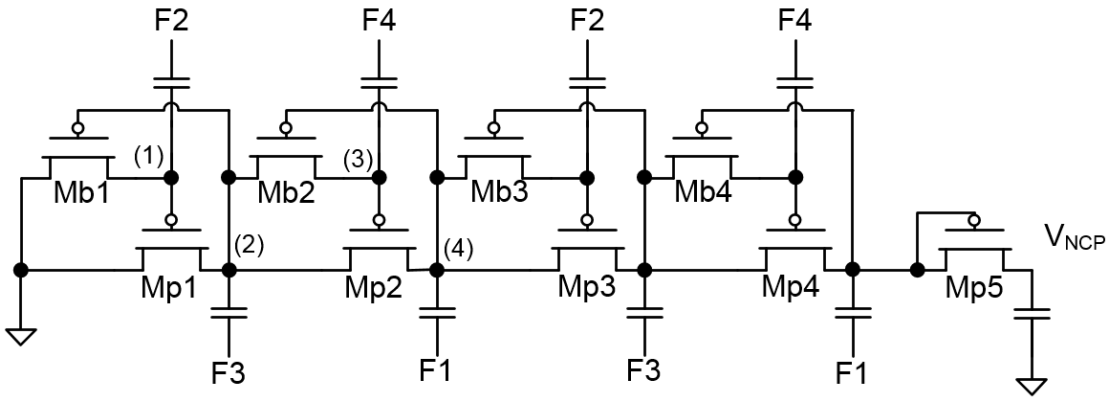


Fig. 2.7 The negative charge pump with PMOS switches.

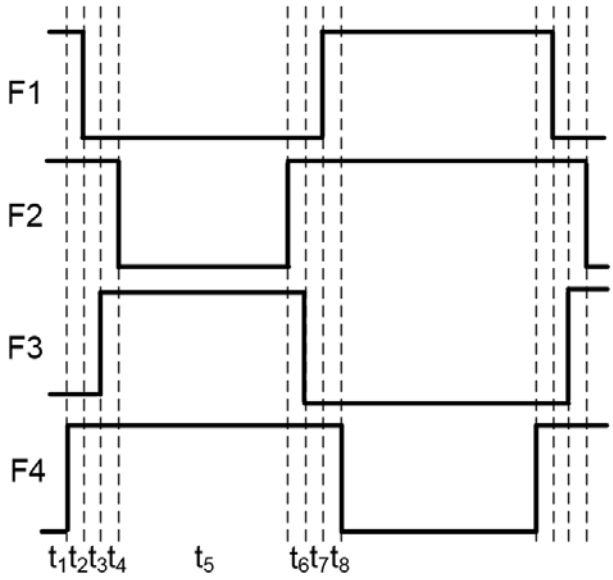


Fig. 2.8 The 4-phase clock scheme of the negative charge pump with PMOS switches.

2.3.2 Cross-Couple Negative Charge Pump

Fig.2.9 is cross-couple negative charge pump [9], which consist of NMOS and PMOS charge transfer switches and pumping capacitor. This charge pump use two non-overlap clock to operate this circuit.

When clk is logic low (clkb is logic high), the voltage of node 1 is dropped to -V_{DD} and the voltage of node 2 is rose to GND, where V_{DD} is the voltage swing of clock. Then, Mn1 is turned on to transfer charge and Mp1 is turned off. Mn2 is turned off and Mp2 is turned on. The voltage of output become -V_{DD}, which is the same as node 1.

Similarly, when clk is logic high (clkb is logic low), the voltage of node 1 is rose to GND and the voltage of node 2 is dropped to -V_{DD}. Then, Mn1 is turned off to and Mp1 is turned on transfer charge. Mn2 is turned on and Mp2 is turned off. The voltage of output become -V_{DD}, which is the same as node 2.

By this operation, the voltage can be pumped to negative high. Moreover, the maximum voltage stress of MOS switches is VDD, which may not cause gate-oxide reliability issues in low voltage CMOS process.

Fig.2.10 is adopted from [9]. In this work, it use three stage charge pump. If the deep N-wells connect to source of PMOS, there is some P-N junctions which shown as Fig.2.10 (a). These junctions may have leakage during circuit operation, which may degrade the efficiency of charge pump or may cause latch-up issues. So, the deep N-wells are connect to ground to prevent this, which depicts as Fig.2.10 (b). However, the PMOS switches may have body effect, which may increase the conduction loss of charge pump.

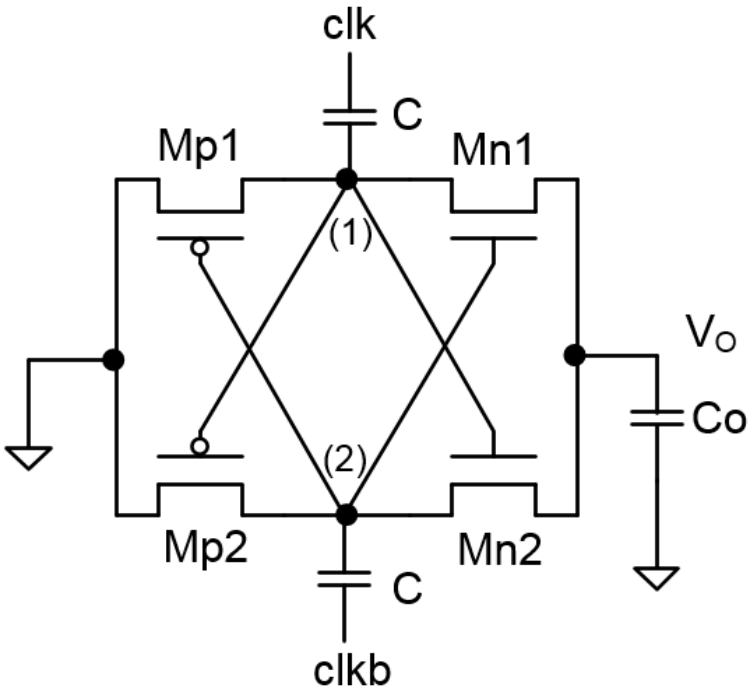


Fig. 2.9 Cross-couple negative charge pump.

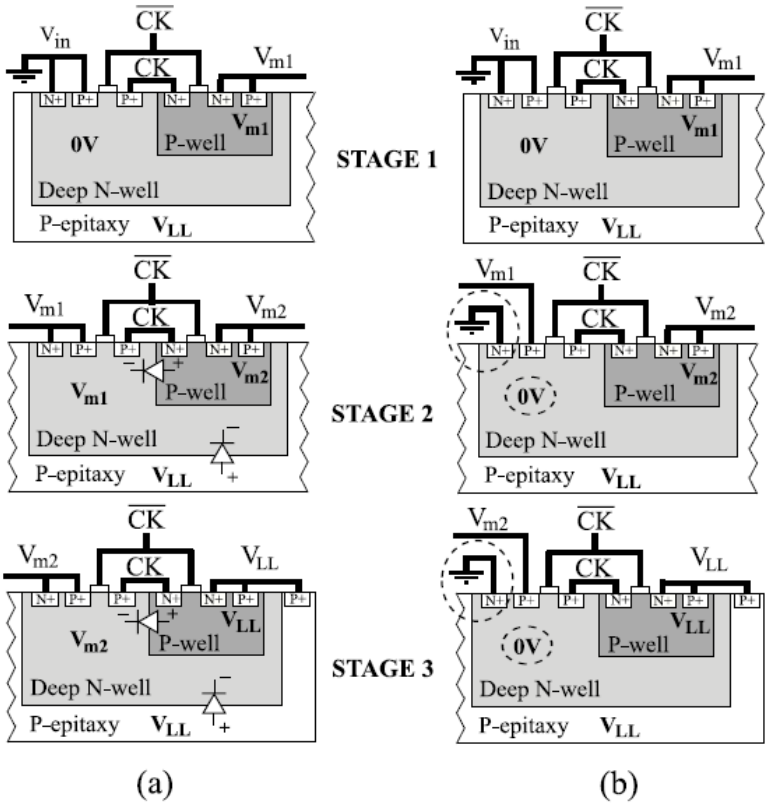


Fig. 2.10 (a) The deep N-well tied to source of PMOS. (b) The deep N-well tied to ground. [9]

2.3.3 4-phase Negative Charge Pump with NMOS Charge Transfer Switches

In triple well process, the PMOS switches of negative charge pump may have body effect, to prevent this, the circuit which depict as Fig.2.11 had been proposed [10]. The charge pump circuit consists of NMOS transfer switches and pumping capacitors. The bulk of NMOS switches can be tied to source without leakage of P-N junctions and latch up issues. Compare to the all PMOS negative charge pump, the last stage doesn't use diode connected MOS, which may not cause forward voltage drop. The clock control scheme is similar to all PMOS negative charge pump. This charge pump use 4-phase clock scheme to control NMOS transfer switches, the 4-phase clock is shown as Fig.2.12.

Here, we separate 4-phase clock to eight intervals. At the interval t_1, the voltage of node 1 is GND and the voltage of node 2 is $-2V_{DD}$, where V_{DD} is the voltage swing of

clock. The voltage of node 3 is V_{DD} and the voltage of node 4 is $-2V_{DD}$. Mn1 and Mb2 are turned on, and Mb1 and Mn2 are turned off.

At the interval t_2, the voltage of clk1 is dropped to low (GND). The voltage of node 3 is dropped to GND to cut off Mn1. The voltage of node 1, node 2 and node 4 are the same as the voltage at interval t_1. Mb1 and Mn2 keep being turned off and Mb1 keep being turned on.

At the interval t_3, the voltage of clk2 is rose to high (V_{DD}) to turn on Mb1. The voltage of node 2 is rose to $-V_{DD}$ and the voltage of node 4 is rose to $-V_{DD}$ as well. The voltage of node 1 and node 3 are the same as the voltage at time interval t_2. Mn1 and Mn2 keep being turned off to prevent leakage current from the front stage and Mb2 keep being turned on.

At the interval t_4, the voltage of clk3 is dropped to low (GND). The voltage of node 1 is dropped to $-V_{DD}$ to cut off Mb2 and the voltage of node 3 is dropped to $-V_{DD}$ as well. The voltage of node 2 and node 4 are the same as the voltage at time interval t_3. Mn1 and Mn2 keep being turned off and Mb1 keep being turn on to cut off Mn1.

At the interval t_5, the voltage of clk4 is rose to high (V_{DD}). The voltage of node 4 is rose to GND to turn on Mn2, and the voltage of node 1 and node 2 become $-V_{DD}$. The voltage of node 3 keep $-V_{DD}$. Mn1 and Mb2 keep being turned off and Mb1 keep being turn on to cut off Mn1.

At the interval t_6, the voltage of clk4 is dropped to low (GND). The voltage of node 4 is dropped to -VDD to cut off Mn1. The voltage of node1, node 2 and node 3 are the same as the voltage at time interval t_5. Mn1 and Mb2 keep being turned off and Mb1 keep being turn on to cut off Mn1.

At the interval t_7, the voltage of clk3 is rose to high (V_{DD}). The voltage of node 1 is rose to GND to turn on Mb2 and the voltage of node 3 is rose to GND as well. The

voltage of node 2 and node 4 are the same as the voltage at time interval t_6. Mn1 and Mn2 keep being turned off and Mb1 keep being turned on.

At the interval t_8, the voltage of clk2 is dropped to low (GND) to turn off Mb1. The voltage of node 2 and node 4 are dropped to $-2V_{DD}$. The voltage of node1 and node 3 are the same as the voltage at time interval t_7. Mn1 and Mn2 keep being turned off to prevent leakage and Mb1 keep being turned on.

By these operations, the output voltage can be pumped to negative high voltage without body effect. The advantage of this pump is no leakage current by 4-phase scheme. However, the maximum voltage stress on NMOS is as high as 2VDD, which may cause gate-reliability issues in low voltage CMOS process.

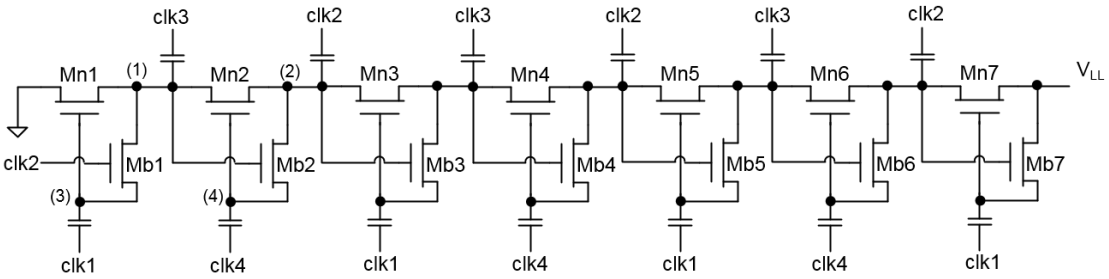


Fig. 2.11 Negative charge pump with NMOS switches.

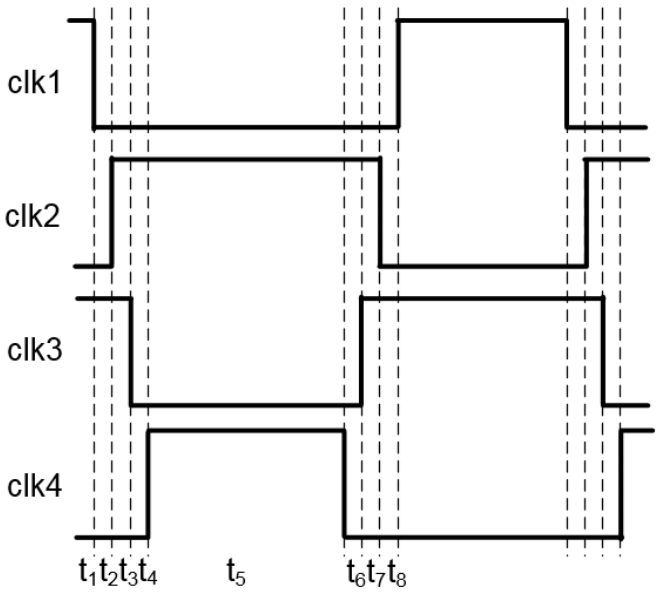


Fig. 2.12 4-phase clock control scheme of the negative charge pump with NMOS switches.

Chapter 3

Design of Positive Charge Pump Regulator with Low Input Peak Current

3.1 Design of Positive Charge Pump Regulator

3.1.1 Circuit Block Diagram of Proposed Positive Charge Pump Regulator

The proposed charge pump regulator consists of error amplifier, phase shift clock generator, level shifter, 4-phase clock generator and 3-stage charge pump, as shown in Fig. 3.1. For the charge pump, the higher output voltage is, the higher clock frequency should be. Therefore, the proposed charge pump used the PFM feedback to generate regulated output voltage V_{CC} [11]~[12]. The PFM feedback consist of voltage divider, error amplifier and voltage control oscillator (VCO). The PFM feedback consists of voltage divider, error amplifier and voltage control oscillator (VCO). The output voltage (V_{ctrl}) of amplifier is adjusted by the voltage difference between V_{FB} and V_{REF}. The clock frequency of clkl is controlled by V_{ctrl}. When V_{CC} is lower than 11V, controlled voltage (V_{ctrl}) become higher and the frequency of clkl arise until V_{CC} = 11V. In contrast, when V_{CC} is higher than 11V, controlled voltage (V_{ctrl}) become lower and the frequency of clkl become slower until V_{CC} = 11V. The 4-phase clock generator provides the charge pump with the adaptive control signals. The phase shift clock generator can generate clkd_1, clkd_2 and clkd_3. When control signal V_{ctrlp} is logic low, the clock waveforms of clkd_1, clkd_2 and clkd_3 depict as Fig. 3.2 (a). Otherwise, when control signal V_{ctrlp} is logic high, the clock waveforms of clkd_1, clkd_2 and clkd_3 depict as Fig. 3.2 (b). The peak current from V_{DDH} can be reduced by the three phase shift clock waveforms. Lower peak current from V_{DDH} may improve transient

response of the dc regulator which provide V_{DDH} to charge pump, and can inject less noise into other circuit in biomedical SoC [13].

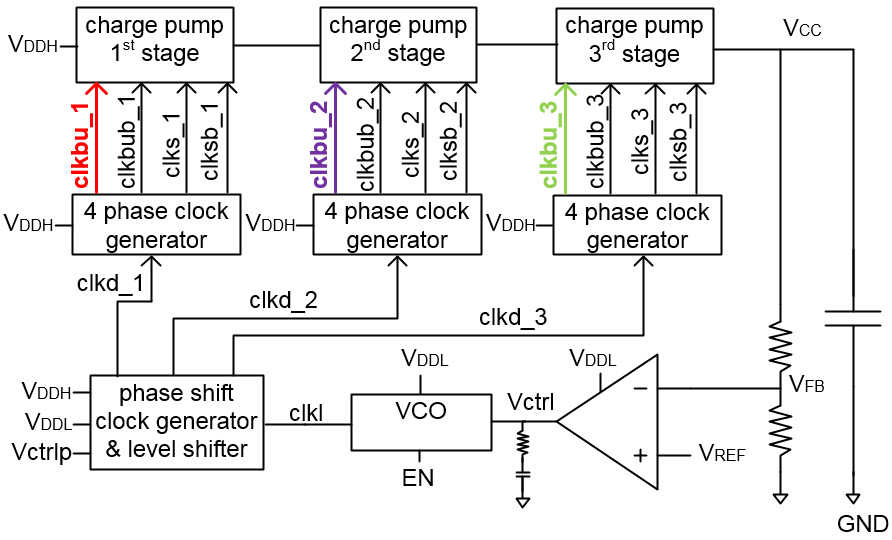
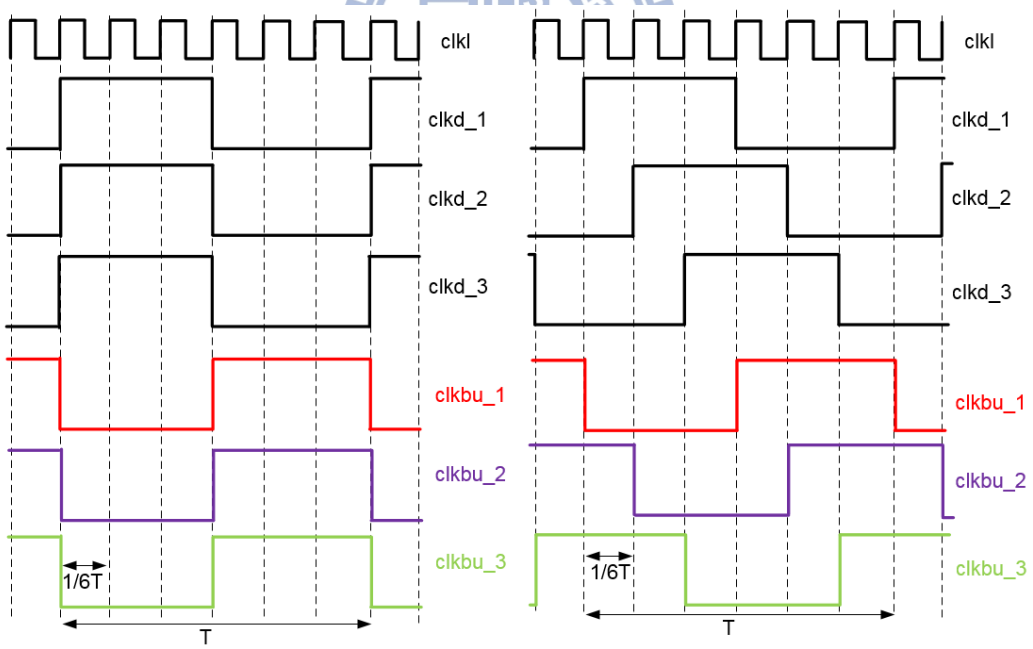


Fig. 3.1 The proposed charge pump regulator consists of error amplifier, phase shift clock generator, level shifter, 4 phase clock generator, and 3 stage charge pump.



(a) (b)

Fig. 3.2 (a) The clock waveform of clkd_1, clkd_2, and clkd_3 when V_{ctrlp} is logic high. (b) The clock waveform of clkd_1, clkd_2, and clkd_3 when V_{ctrlp} is logic low.

Fig. 3.3 depicts a 4-phase cross couple charge pump. It shows the current flow from V_{DDH} when clock signal clkbub is high. Fig. 3.4 (a) depicts the waveform of current flow when control signal V_{ctrlp} is low. Because MOS like resistance when it is in triode region, the waveform of current flow likes RC discharge circuit. Fig. 3.4 (b) depicts the waveform of current flow when control signal V_{ctrlp} is high. The peak current in Fig. 3.4 (b) is lower than the peak current in Fig. 3.4 (a).

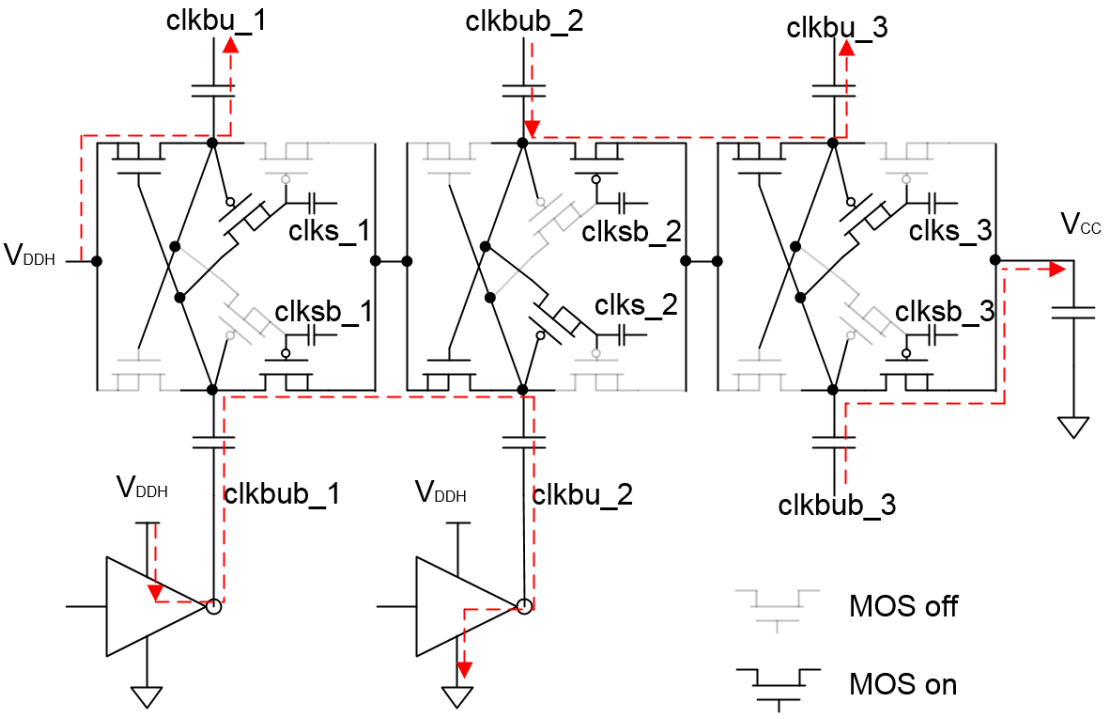


Fig. 3.3 Current flow when clkbub is V_{DDH}.

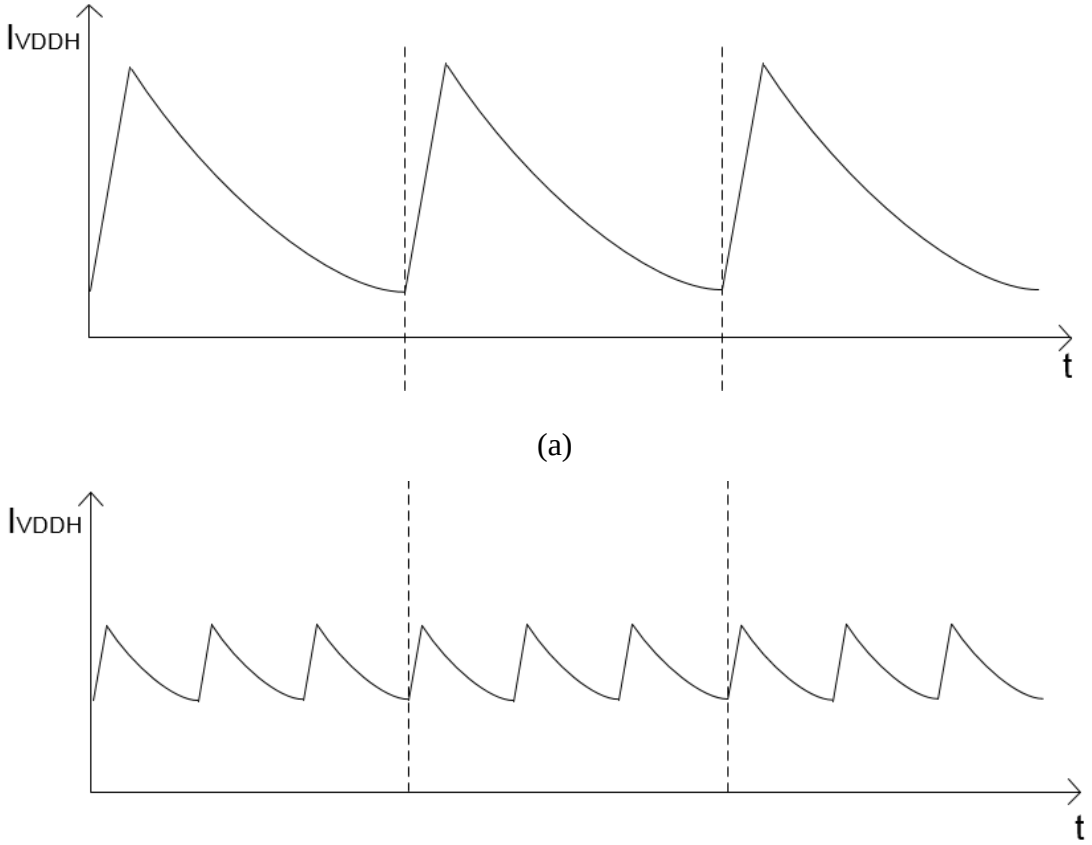


Fig. 3.4 (a) Current flow from V_{DDH} when V_{ctrlp} logic low. (b) Current flow from V_{DDH} when V_{ctrlp} is logic high.

3.1.2 Charge Pump Circuit and 4-phase Clock Generator

Fig. 3.5 shows the 3-stage charge pump. It can output high voltage level without the issues of electrical overstress and gate-oxide reliability [14]. Compare to conventional two phase cross-couple charge pump, this 4-phase cross-couple charge pump can reduce the return-back leakage current. Therefore, this pump has higher efficiency and higher pumping gain than conventional charge pump. Fig. 3.6 shows the 4-phase clock waveforms and Fig. 3.7 shows the circuit of 4-phase clock generator.

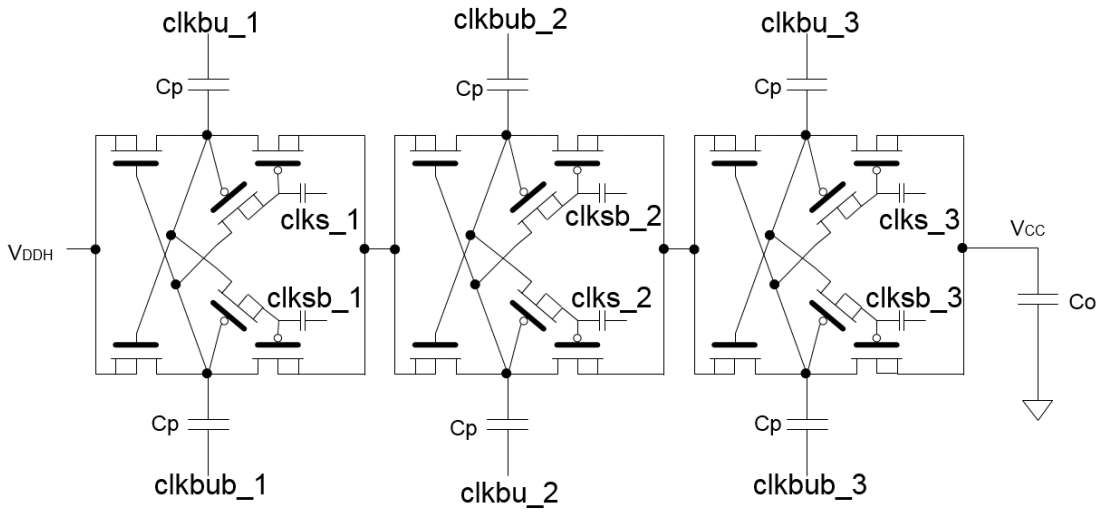


Fig. 3.5 The circuit of 3-stage charge pump.

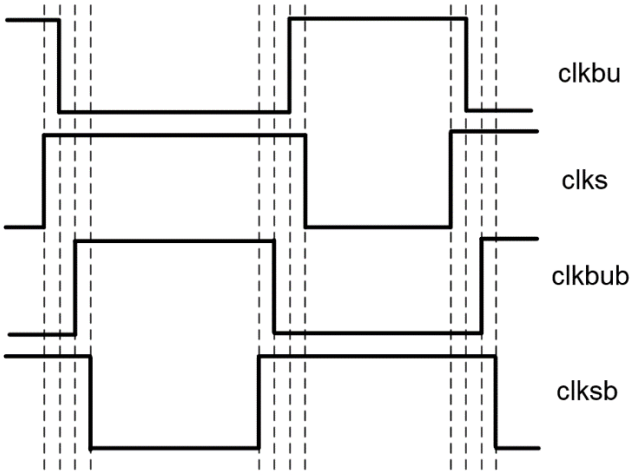


Fig. 3.6 4-phase clock waveforms which is generated from 4-phase clock generator.

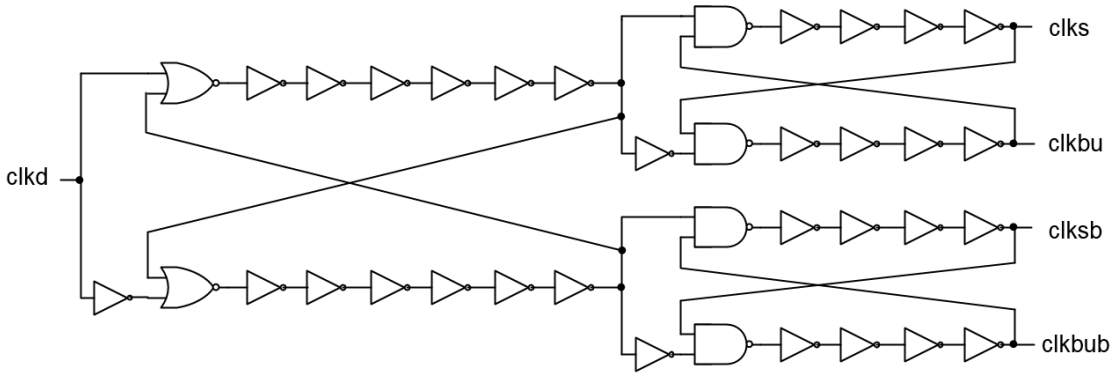


Fig. 3.7 4-phase clock generator.

3.1.3 Bandgap Reference, Error Amplifier, VCO and Phase Shift Clock Generator

Fig. 3.8 shows the bandgap reference [15], which generate reference voltage V_{REF} to error amplifier. Fig. 3.9 shows the error amplifier [16]. Fig. 3.10 shows the current starve voltage control ring oscillator. The first stage of VCO is nand gate which provide the initial condition for VCO.

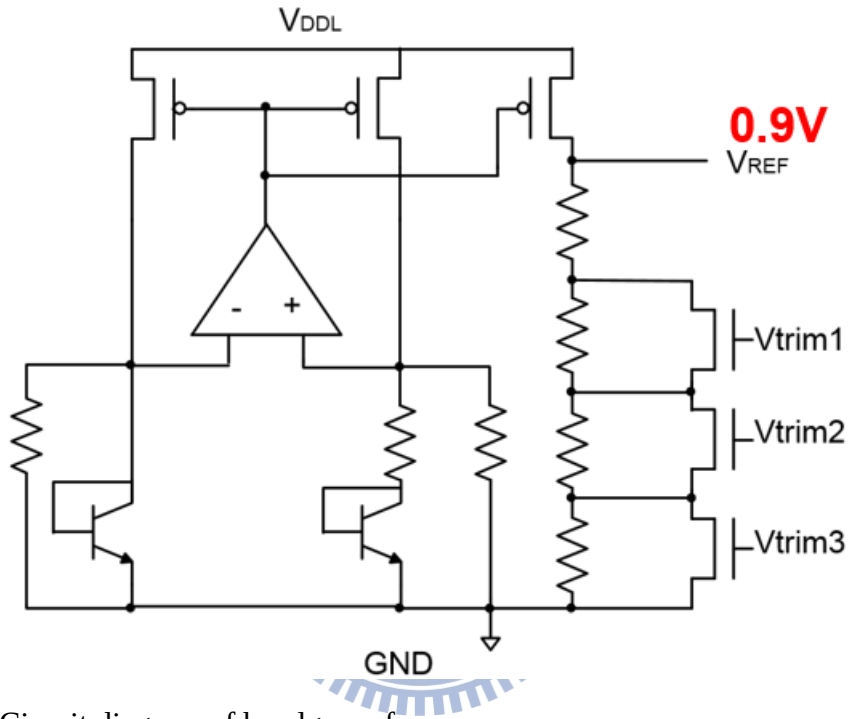


Fig. 3.8 Circuit diagram of bandgap reference.

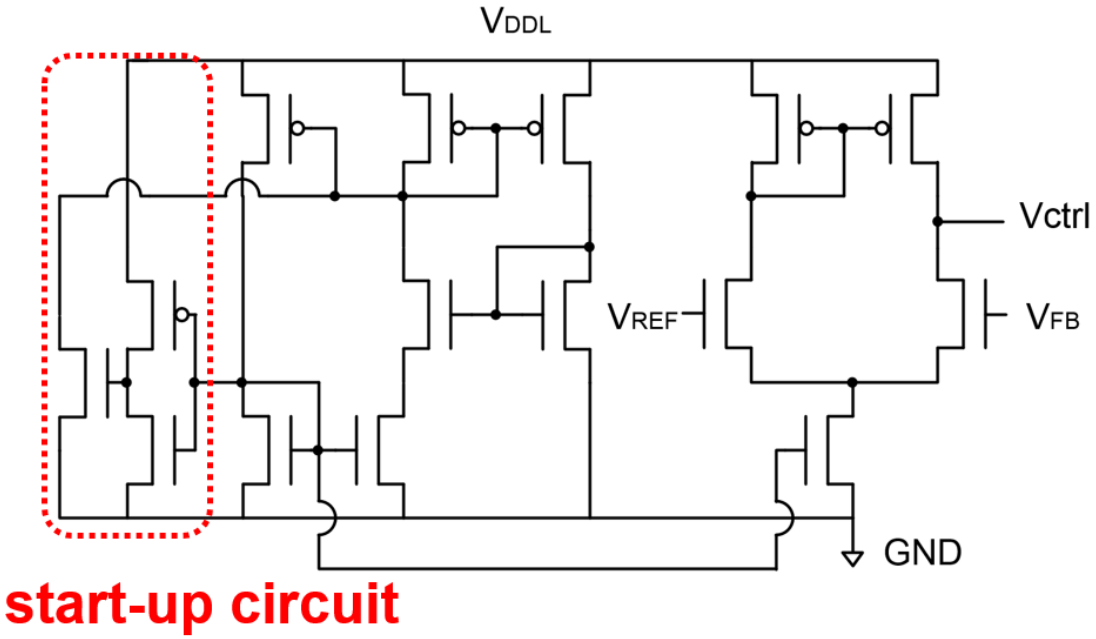


Fig. 3.9 Circuit diagram of error amplifier.

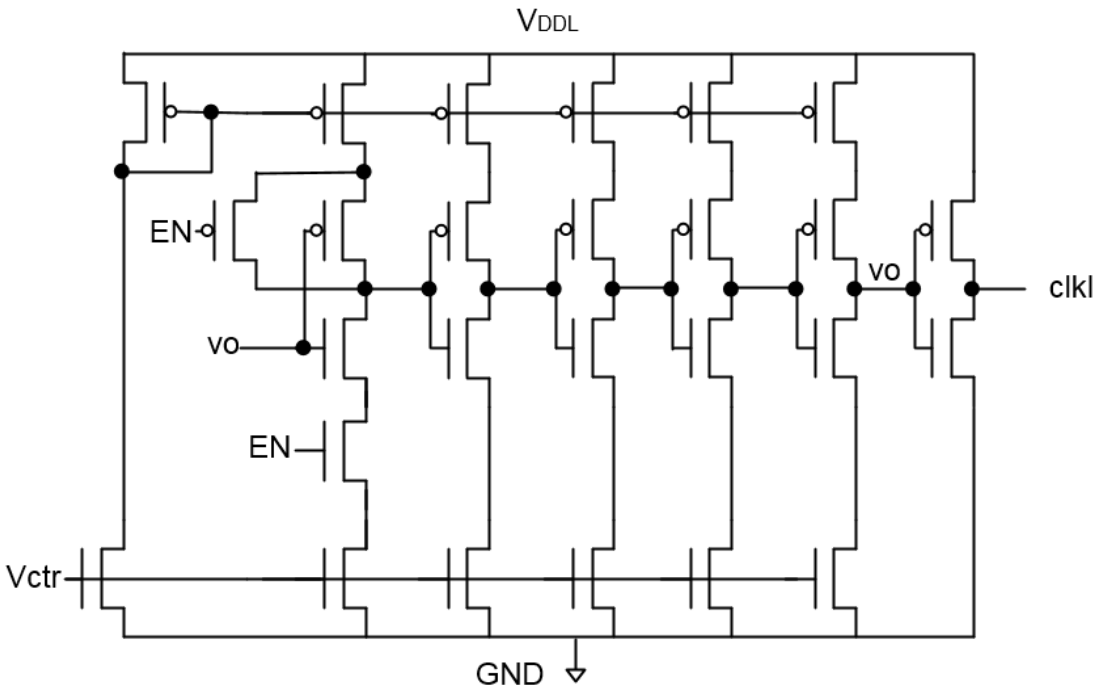


Fig. 3.10 Circuit diagram of current starve voltage control ring oscillator.

Fig. 3.11 shows the circuit diagram of phase shift clock generator and level shifter. The level shifter can transfer 1.8V clock signal to 3.3V clock signal. When control signal V_{ctrlp} =1, the output clock signal (clkd_1, clkd_2 and clkd_3) have phase shift like Fig. 3.2. When control signal V_{ctrlp}=0, the output clock signal (clkd_1, clkd_2 and clkd_3) don't have phase shift. It means that the waveform of clkd_1, clkd_2 and clkd_3 are the same.

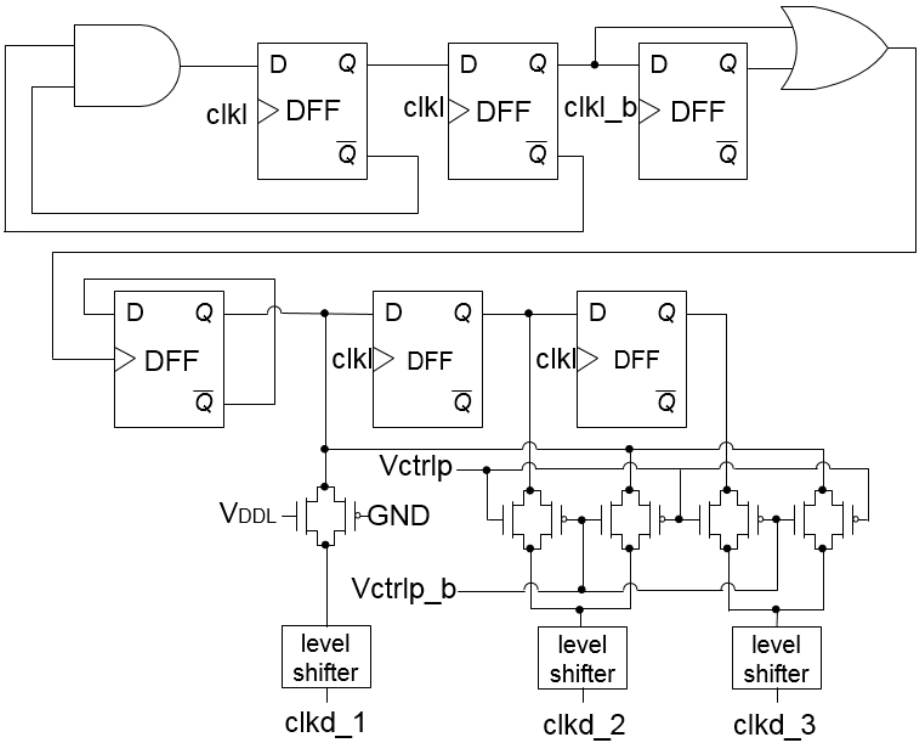
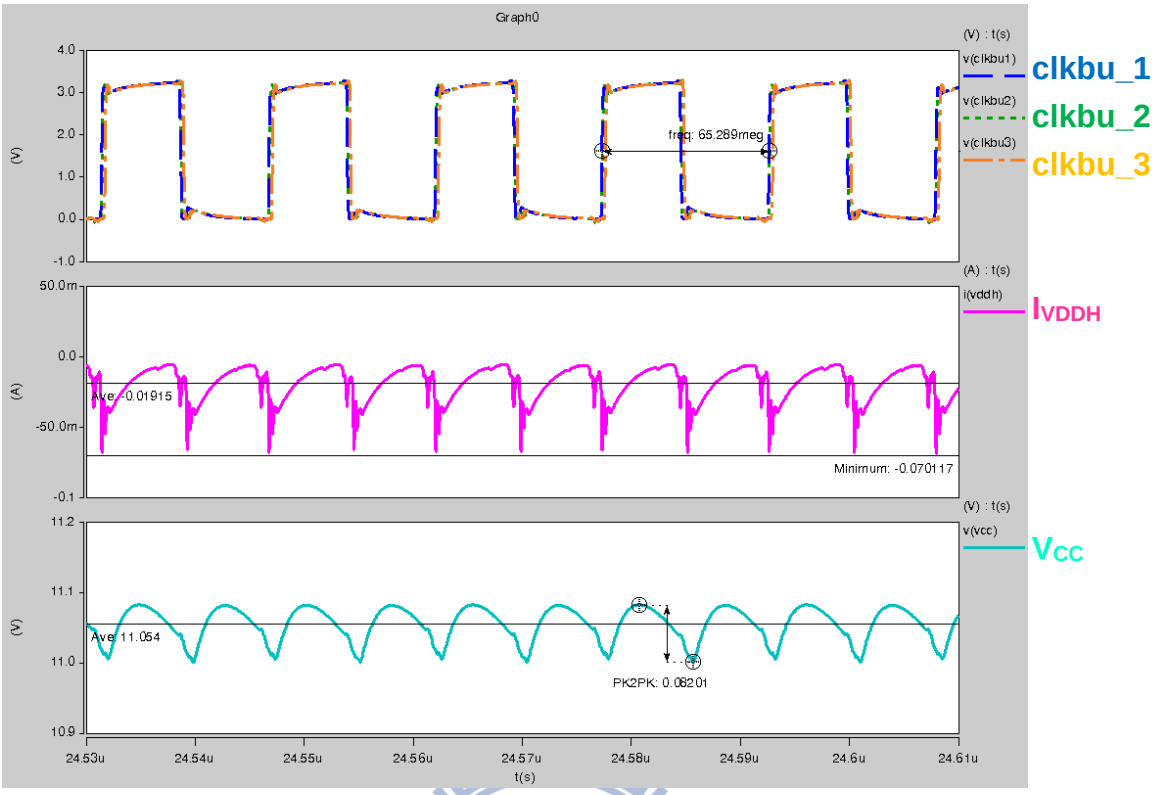


Fig. 3.11 Circuit diagram of phase shift clock generator and level shifter.

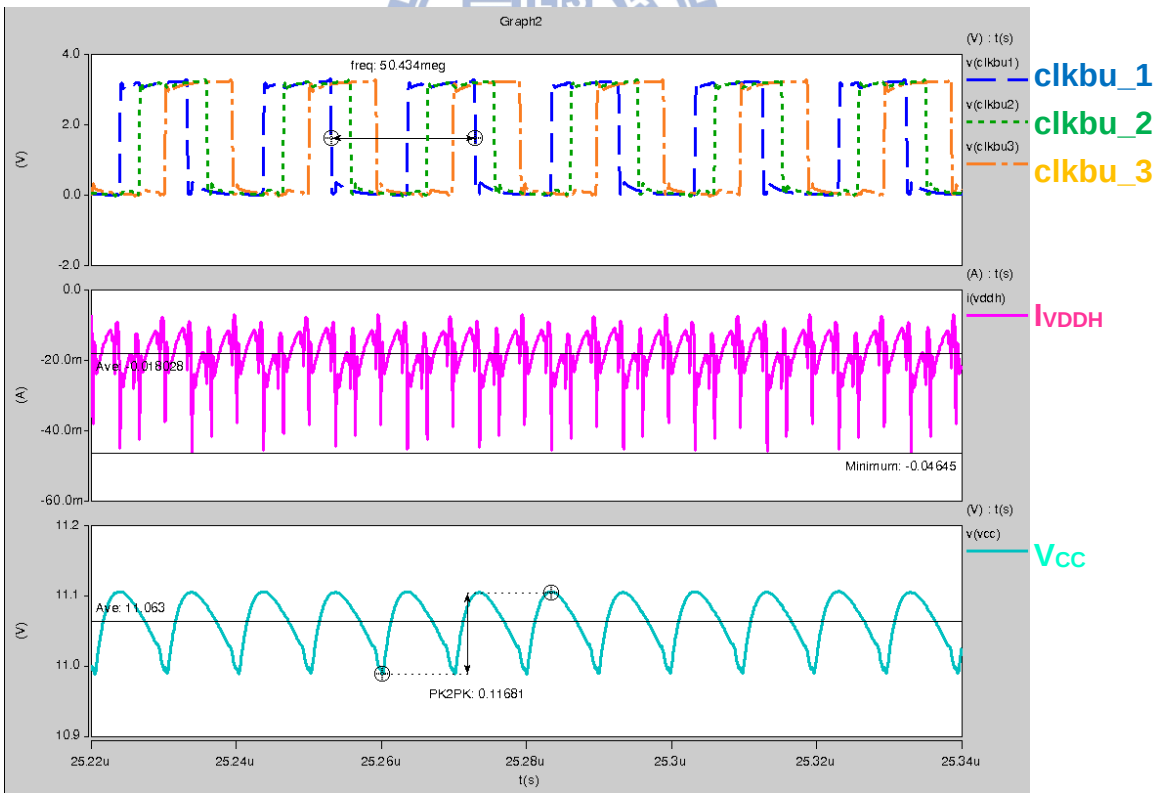
3.2 Simulation Results

This work have been simulated in HSPICE with TSMC 0.18-μm 1.8-V/3.3-V CMOS process. Fig. 3.12 (a) depicts the simulation result of charge pump when V_{ctrlp}=0 and I_{load}=3.5mA. The clock signals (clkbu_1, clkbu_2, and clkbu_3) charge pump don't have phase shift. The pumping frequency is 65.28MHz. The input peak current ($I_{VDDH(max)}$) is 70mA and the average output voltage (V_{CC}) is about 11.054V. The efficiency of charge pump is 61.5%.

Fig. 3.12 (b) depicts the simulation result of charge pump when V_{ctrlp}=1 and I_{load}=3.5mA. The clock signals (clkbu_1, clkbu_2, and clkbu_3) charge pump have phase shift. The pumping frequency is 50.43MHz. The input peak current ($I_{VDDH(max)}$) is 46mA and the average output voltage (V_{CC}) is about 11.063V. The efficiency of charge pump is 65.68%. As the simulation result, we can reduce the input peak current with phase shift clock control.



(a)



(b)

Fig. 3.12 Simulation results of charge pump when (a)V_{ctrlp}=0 and I_{load}=3.5mA (b)V_{ctrlp}=1 and I_{load}=3.5mA.

3.3 Measurement Results

This work have been fabricated in TSMC 0.18-μm 1.8-V/3.3-V CMOS process. The charge pump aims to output voltage 11V and maximum current 3.5mA. The pumping capacitors (C_P) of charge pump are 50pF and the output capacitor (C_O) is 100pF. All capacitors of the positive charge pump are fully on-chip. Fig. 3.13 depicts the die photo of test chip, which includes the 3-stage charge pump and 4-phase clock generator (A), output capacitor of charge pump (B), and bandgap reference, VCO, error amplifier and phase shift clock generator (C). The test chip area is 1.87 x 1.48mm^2.

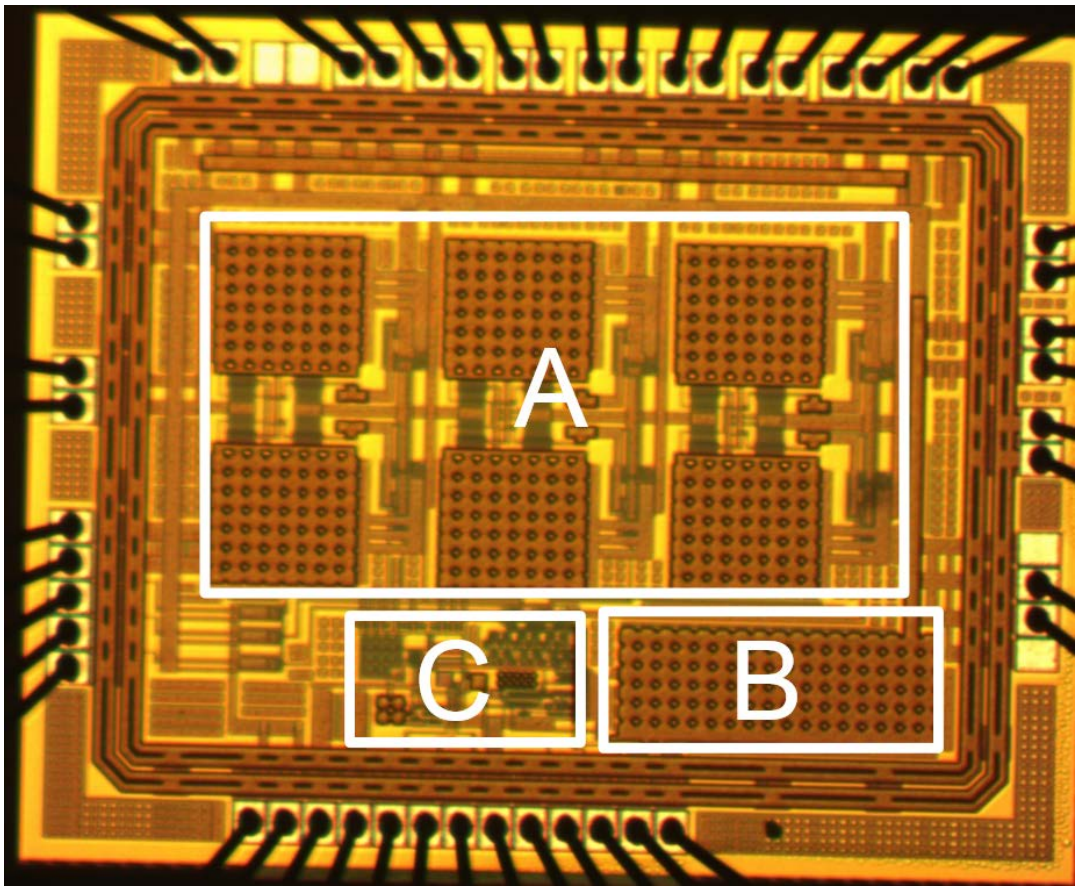
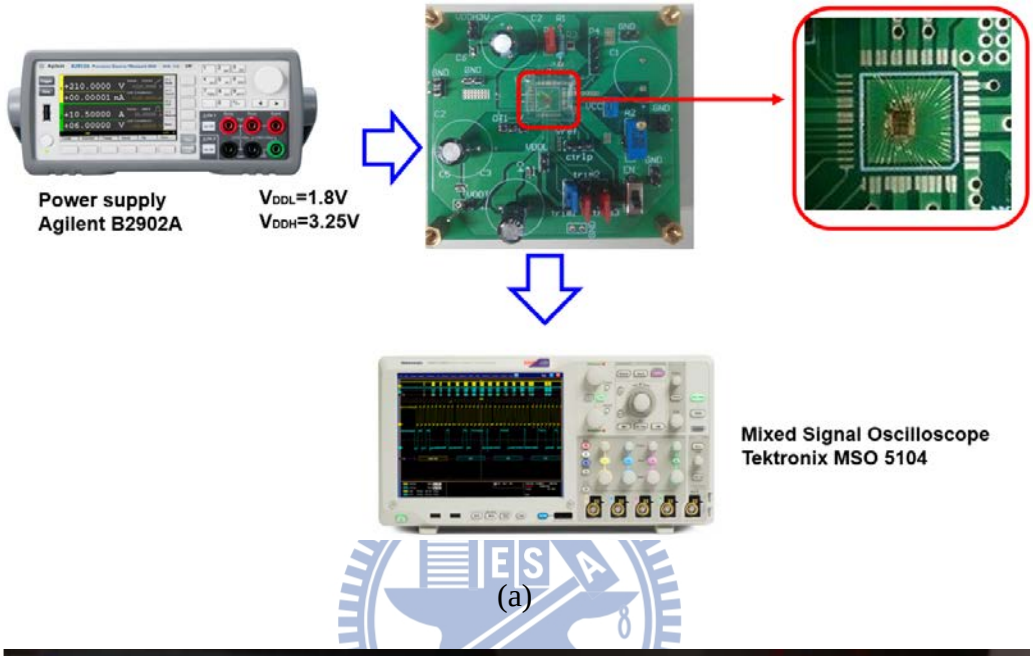
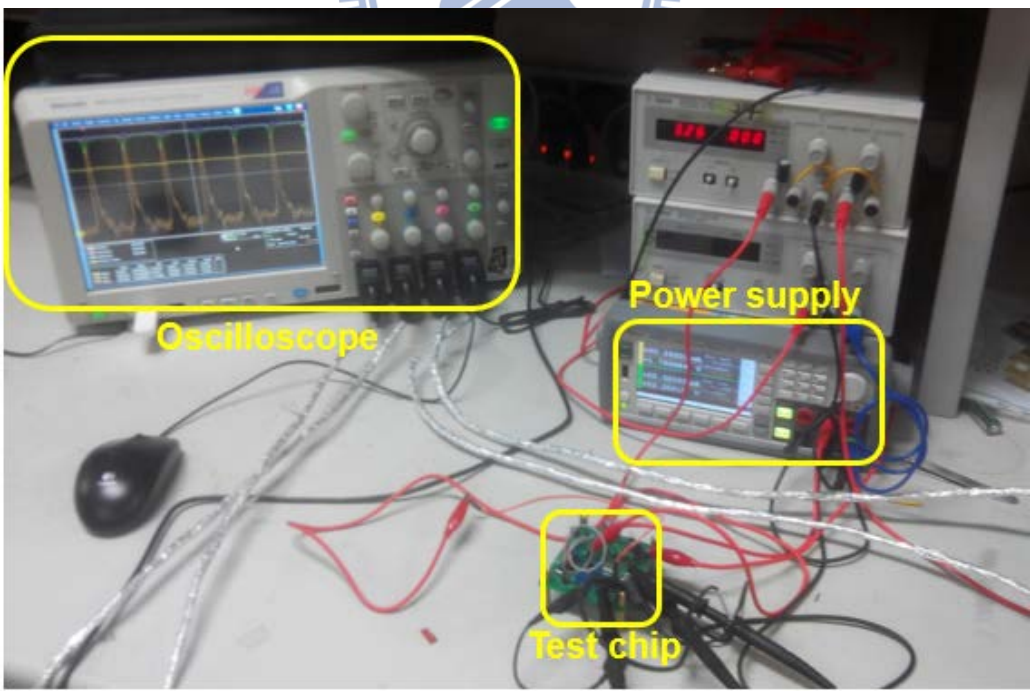


Fig. 3.13 Die photograph with A: 3-stage charge pump and 4-phase clock generator, B: output capacitor of charge pump, and C: bandgap reference, VCO, error amplifier and phase shift clock generator.

Fig. 3.14 (a) shows the measurement setup. Agilent B2902A is used to provide voltage 1.8V V_{DDL} and 3.25V V_{DDH}, which is also used to measurement power consumption of the charge pump. Tektronix MSO 5104 is used to observe the waveforms of the charge pump. Fig. 3.14 (b) shows the measurement environment.



(a)



(b)

Fig. 3.14 (a) Measurement setup of power supply, oscilloscope and test chip. (b) Measurement environment.

Fig. 3.15 depicts the measurement result of power on time at I_{load} is 3.5mA and V_{ctrlp} is logic 1, which is about 532nsec. Fig. 3.16 depicts the waveforms to check the phase shift clock generator function. V_{ctrlp}=0 means the clock signal of each stage doesn't have phase shift. V_{ctrlp}=1 means the clock signals of each stage has phase shift. The signals OT1, OT2 and OT3 are generated by clkd_1, clkd_2 and clkd_3 via some buffers respectively. As the measurement result, the function of phase shift clock generator is working.

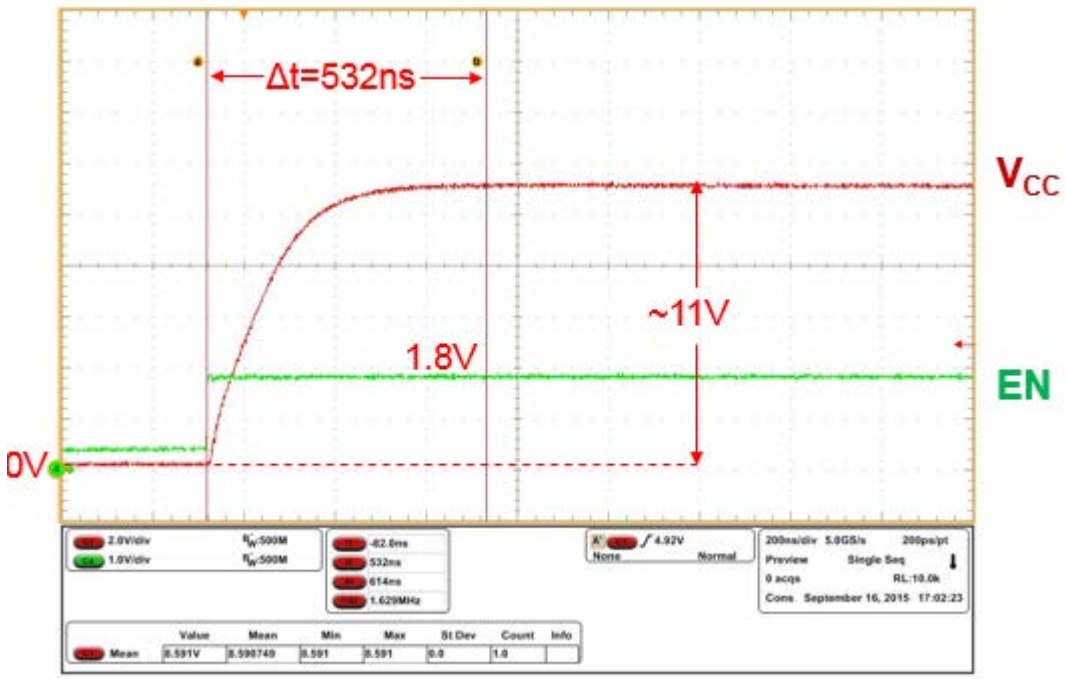


Fig. 3.15 The measurement result of power on time.

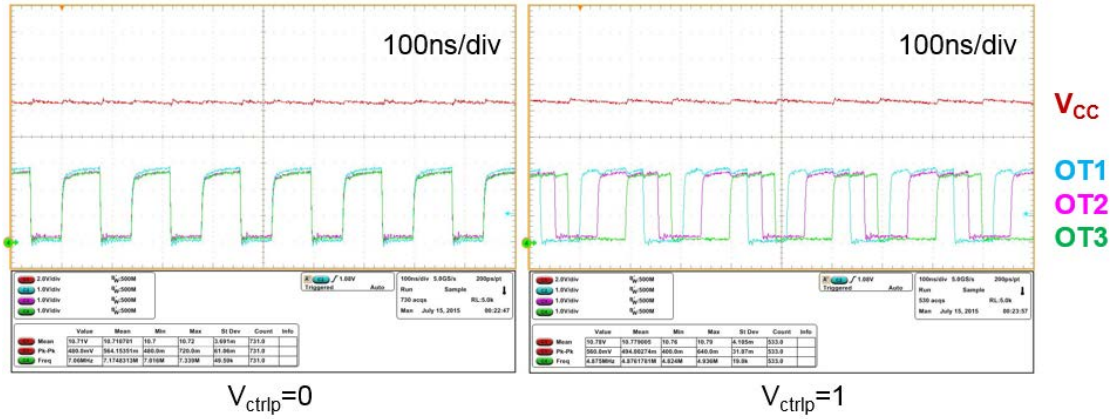


Fig. 3.16 Waveforms of OT1, OT2 and OT3 when I_{load} is 0.5mA.

Fig. 3.17 depicts the measurement result of V_{CC} when I_{load} is 3.5mA. The efficiency is calculated by Eq. (3.1), where P_{VCC} is the power of V_{CC}.

$$\text{Efficiency} = \frac{P_{VCC}}{P_{VDDH}+P_{VDDL}} \tag{3.1}$$

When V_{ctrlp} is logic low (V_{DDL}), the average voltage of V_{CC} is 10.753V. The efficiency of charge pump is 64.32%. The ripple of V_{CC} is about 191.027mV.

When V_{ctrlp} is logic high (V_{DDL}), the average voltage of V_{CC} is 10.812V. The efficiency of charge pump is 67.84% when I_{load} is 3.5mA. The ripple of V_{CC} is about 192.54mV.

Fig. 3.18 shows the measurement result of output voltage (V_{CC}) versus different loading current (I_{load}). Fig. 3.19 shows the measurement result of efficiency versus different loading current (I_{load}). Fig. 3.20 shows the measurement result of output ripple versus different loading current (I_{load}).

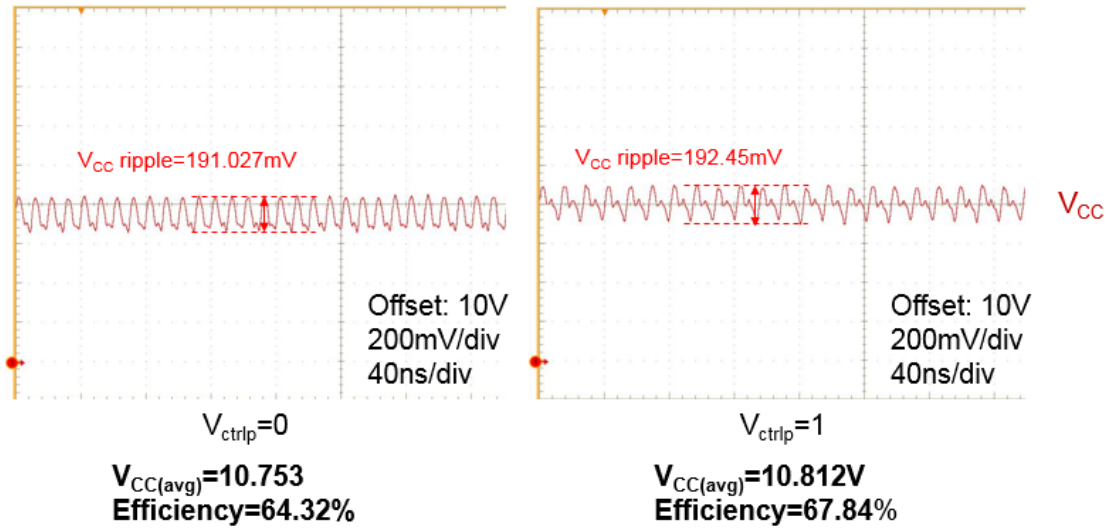


Fig. 3.17 The measurement result of output voltage (V_{CC}) when I_{load} is 3.5mA

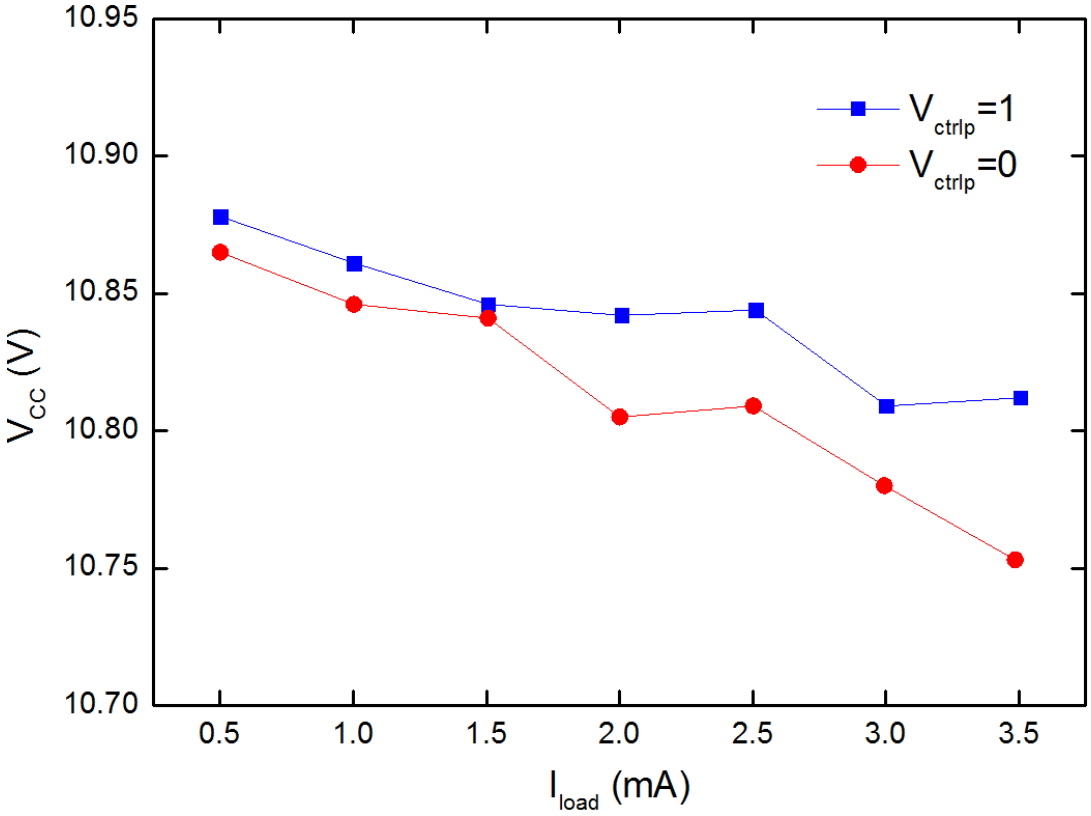


Fig. 3.18 The measurement result of output voltage (V_{CC}) versus different loading current (I_{load}).

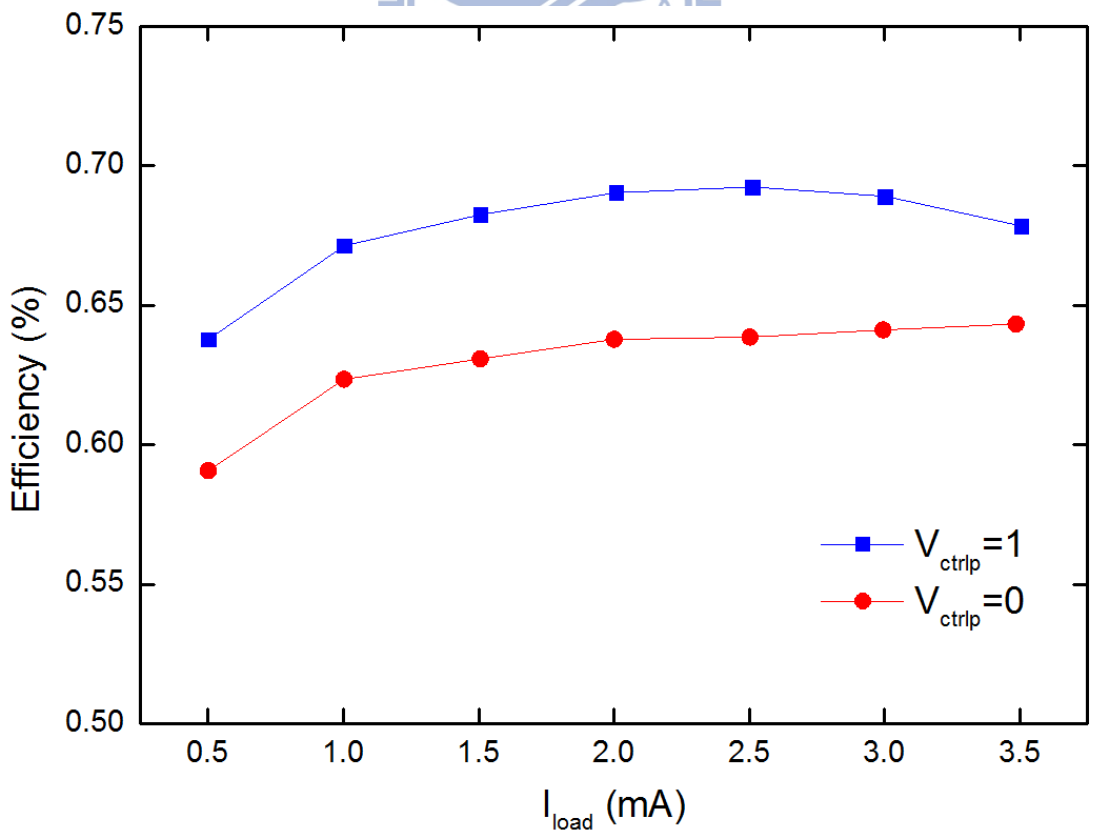


Fig. 3.19 The measurement result of efficiency versus different loading current (I_{load}).

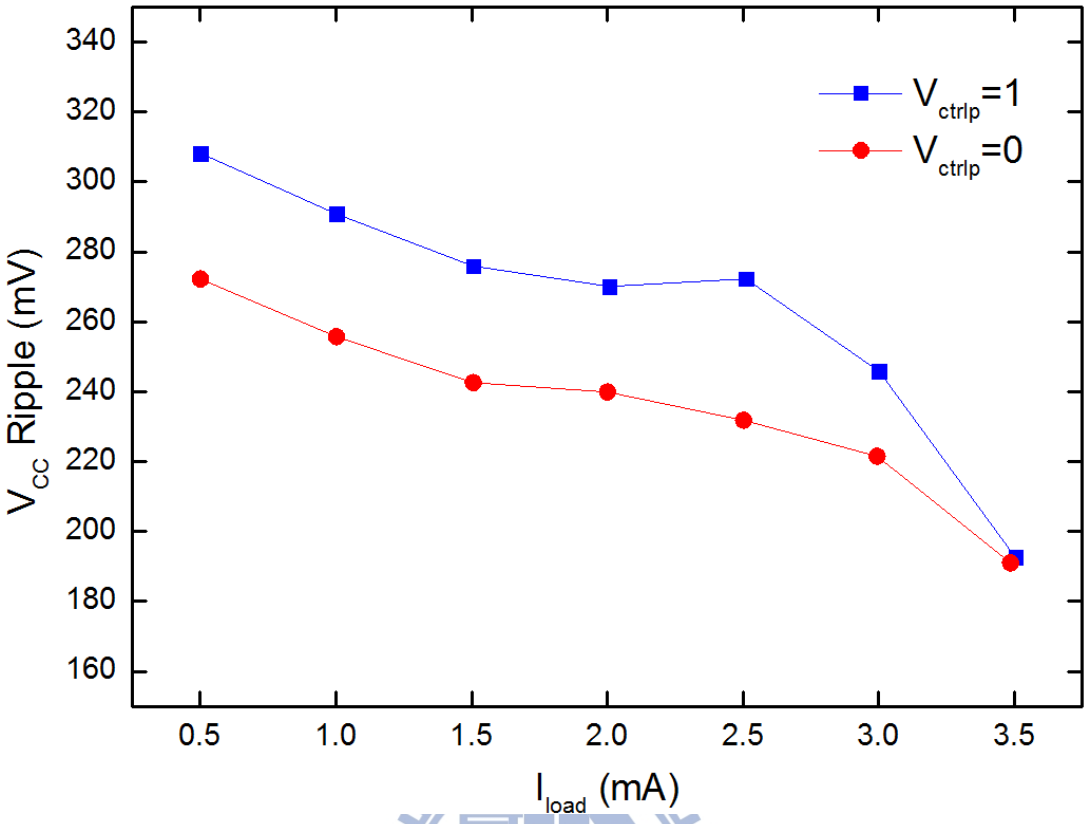


Fig. 3.20 The measurement result of output ripple versus different loading current (I_{load}).

In order to measurement input peak current ($I_{VDDH(max)}$) from V_{DDH}, we add a 5Ω resistance between node V_{DDH2} and V_{DDH} and measure the voltage difference between V_{DDH2} and V_{DDH}. Fig 3.21 shows the measurement setup. Fig. 3.22 depicts the measurement result of input current (I_{VDDH}) from V_{DDH} when I_{load} is 1.5mA. When V_{ctrlp} is logic low (GND), the maximum input peak current ($I_{VDDH(max)}$) is 57.7mA. When V_{ctrlp} is logic high (V_{DDL}), the maximum input peak current ($I_{VDDH(max)}$) is 36.8mA.

Fig. 3.23 depicts the measurement result of input current (I_{VDDH}) from V_{DDH} when I_{load} is 3.5mA. When V_{ctrlp} is logic low (GND), the maximum input peak current ($I_{VDDHmax}$) is 60.7mA. When V_{ctrlp} is logic high (V_{DDL}), the maximum input peak current ($I_{VDDHmax}$) is 31.2mA. Fig 3.24 shows the measurement result of $I_{VDDH(max)}$ versus different loading current in three different chips. In the measurement result, the maximum input peak current can be reduced by applying phase shift clock (clkd_1,

clkd_2 and clkd_3) to the charge pump. Table 3.1 is the comparison of post-simulation and measurement.

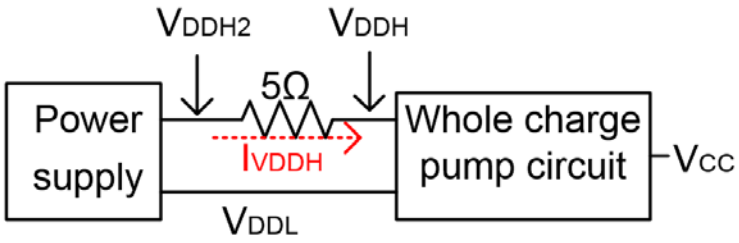


Fig. 3.21 The measurement setup for measuring I_{VDDH}.

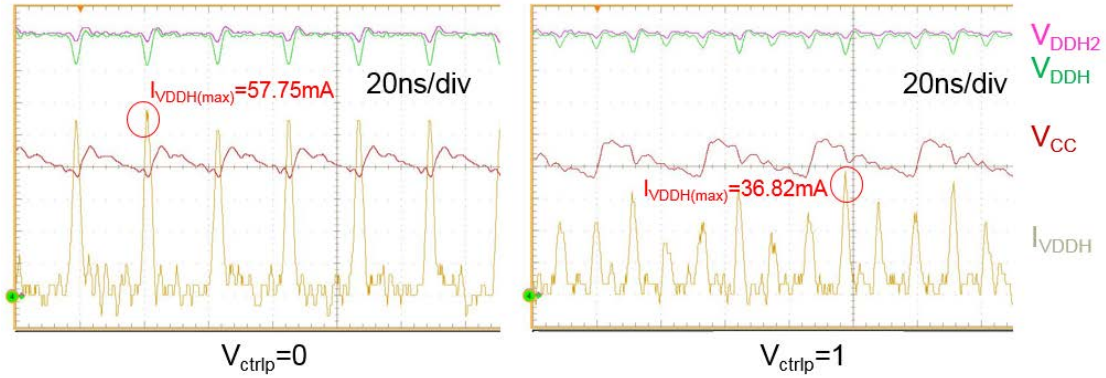


Fig. 3.22 The measurement result of input current (I_{VDDH}) from V_{DDH} when I_{load} is 1.5mA.

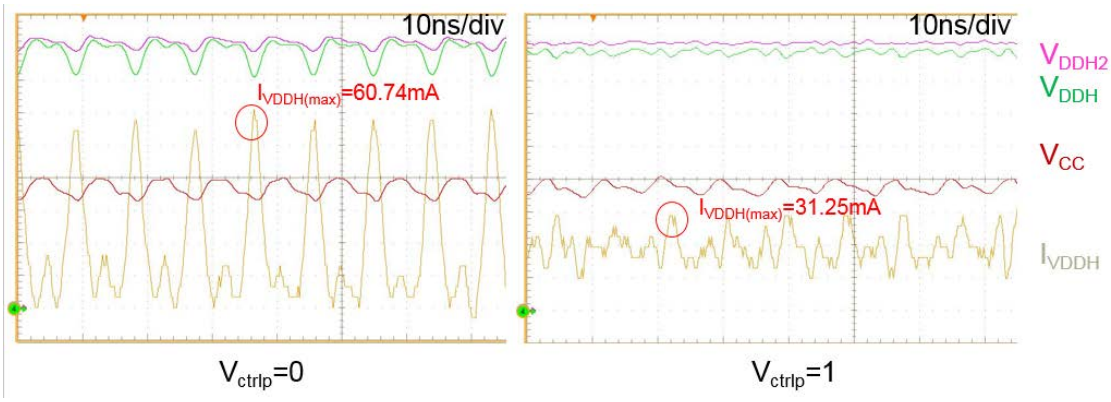


Fig. 3.23 The measurement result of input current (I_{VDDH}) from V_{DDH} when I_{load} is 3.5mA.

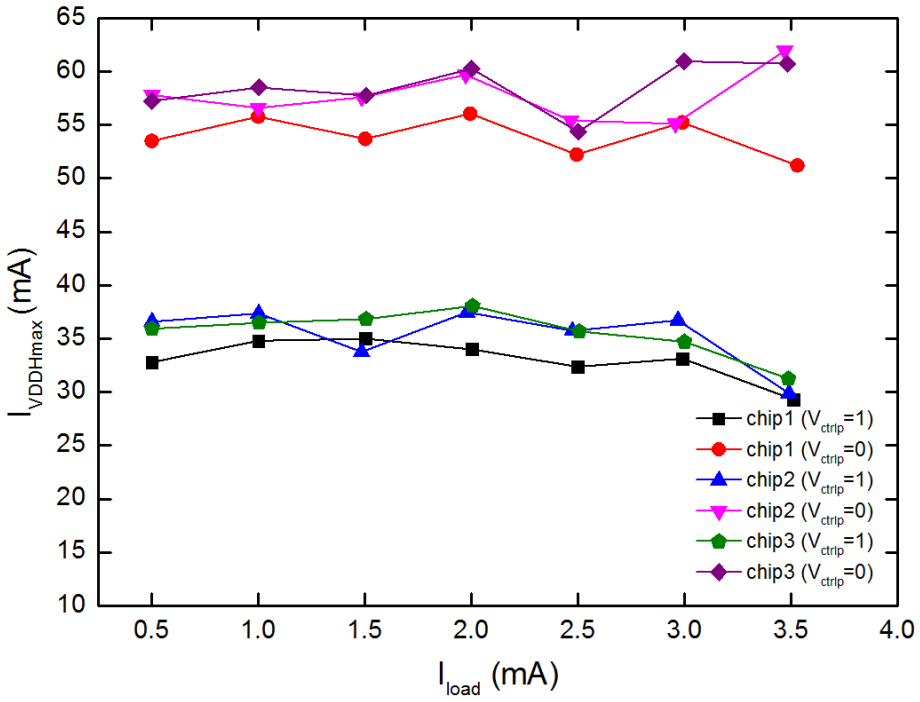


Fig. 3.24 The measurement result of $I_{VDDHmax}$ in three different chip.

Table. 3.1 Comparison of post-simulation and measurement.

		Post-layout simulation (TT)	Measurement
Power supply V_{DDL} / V_{DDH}		1.8V / 3.25V	1.8V / 3.25V
$I_{VDDHmax}$ @ I_{load} = 3.5mA V_{ctrlp} = 0 / V_{ctrlp} = 1		70.11mA / 46.5mA	60.74mA / 31.25mA
V_{CC} / Efficiency (V_{ctrlp} = 1)	0.5mA	11.098V / 66.283%	10.878V / 63.778%
	1mA	11.089V / 68.578%	10.861V / 67.131%
	1.5mA	11.085V / 69.175%	10.846V / 68.246%
	2mA	11.081V / 69.161%	10.842V / 69.04%
	2.5mA	11.076V / 68.683%	10.844V / 69.245%
	3mA	11.069V / 67.703%	10.809V / 68.904%
	3.5mA	11.067V / 65.688%	10.812V / 67.847%
Process		TSMC 0.18μm 1.8V/3.3V CMOS Process	

3.4 Application on Biomedical Stimulation Circuit

In this work, we had used charge pump circuit on cochlear stimulation circuit. Fig. 3.25 depicts the circuit block diagram of cochlear stimulation circuit. All chips had been fabricated in TSMC 0.18-μm 1.8-V/3.3V CMOS process. The charge pump is used in implanted part to generate high voltage to provide stimulator. By measurement, the charge pump can regulate at high voltage and the stimulator can work successfully. The die photo of implanted part is shown as Fig. 3.26, which include A: stimulator driver, B: DSP, C: positive charge pump circuit, D: demodulator and back telemetry, and E: rectifier and regulator. Fig. 3.27 is the measurement result of stimulator and charge pump in cochlear SoC.

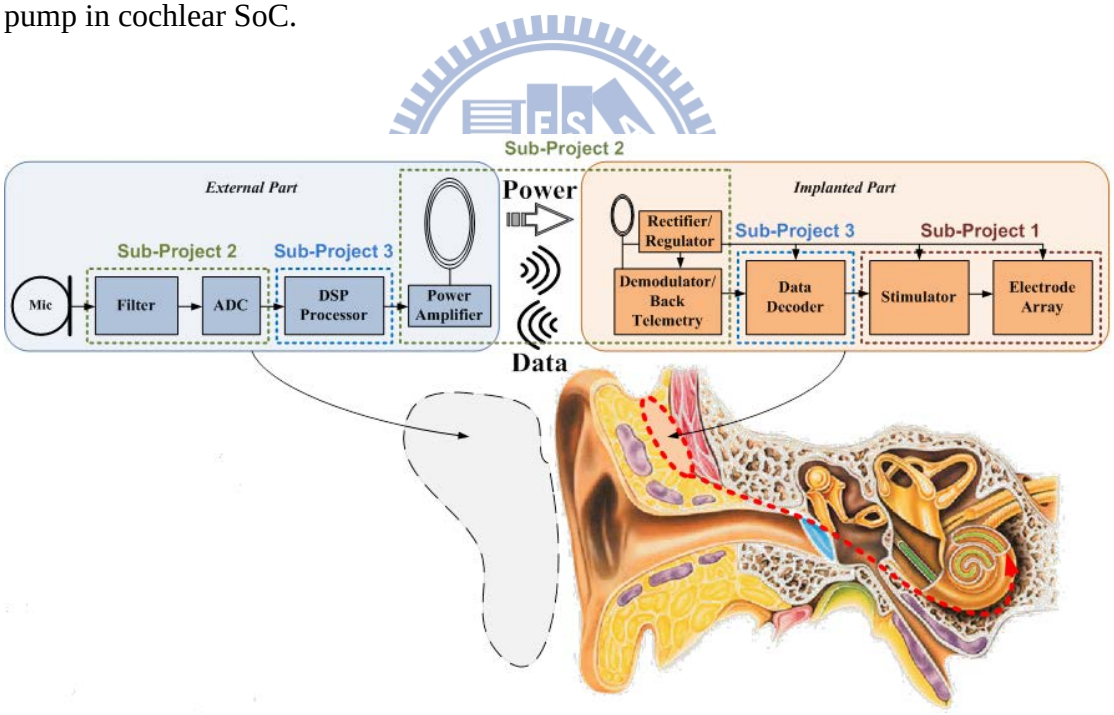


Fig. 3.25 Block diagram of cochlear SoC.

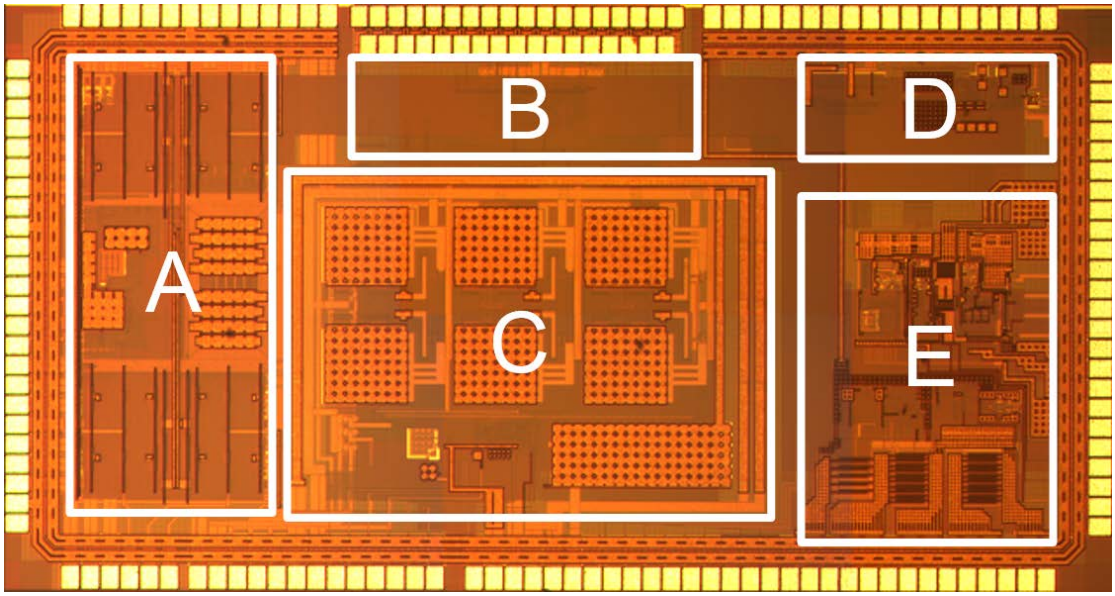


Fig. 3.26 Die photograph with A: stimulator driver, B: DSP, C: positive charge pump circuit, D: demodulator and back telemetry, and E: rectifier and regulator.

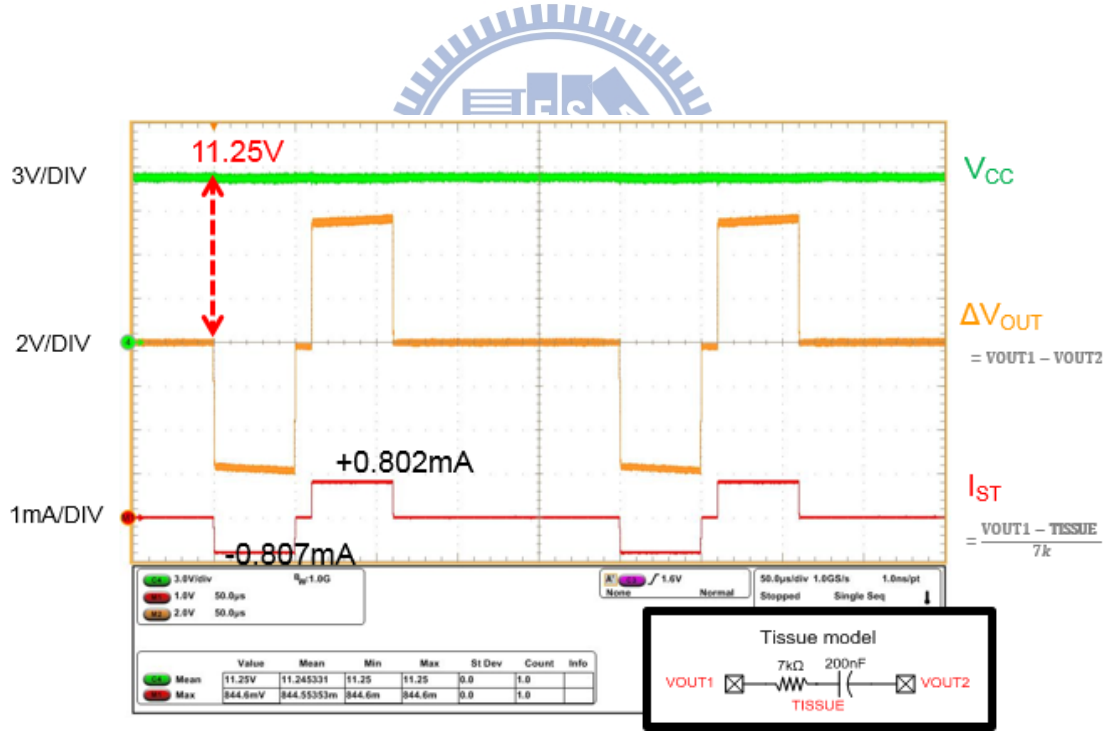
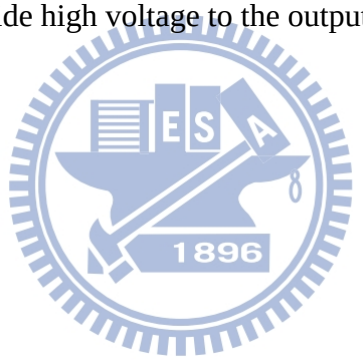


Fig. 3.27 Measurement result of stimulator and charge pump in cochlear SoC.

3.5 Summary

Design of a positive charge pump regulator for biomedical implant is investigated and verified in this chapter. The circuit design have been fabricated in TSMC 0.18-μm 1.8-V/3.3V CMOS process. The proposed design can output 10.8V high voltage and maximum output current 3.5mA without the issues of electrical overstress and gate-oxide reliability. The 4-phase cross couple positive charge pump is used for reducing the return-back leakage current. Each stage of charge pump has its own clock signal which has phase shift different from each other. By the measurement, the clock control scheme can reduce the maximum peak current which flow from power supply V_{DDH}. The function of this charge pump design have been success fully verified in silicon chip, which can successfully provide high voltage to the output load.



Chapter 4

Design of Negative Charge Pump Regulator with Low Input Peak Current

4.1 Design of Negative Charge Pump Regulator

4.1.1 Circuit Block Diagram of Proposed Charge Pump Regulator

The proposed negative charge pump regulator is composed of error amplifier, bandgap reference circuit, voltage-controlled oscillator (VCO), phase shift clock generator, level shifter, 4-phase clock generator and 4-stage negative charge pump, as shown in Fig. 4.1. For the charge pump, when output current become higher, the clock frequency should be higher to keep the voltage level of output voltage. Therefore, the proposed charge pump used the PFM feedback to generate regulated output voltage V_{LL}. The PFM feedback consist of voltage divider, error amplifier and voltage control oscillator (VCO). When the control signal EN of VCO is logic high, VCO start working and charge pump generate negative high voltage V_{LL}. When the control signal EN of VCO is logic low, VCO do not work and the output voltage V_{LL} of charge pump is zero. The output voltage (V_{ctrl}) of amplifier is adjusted by the voltage difference between V_{FB} and V_{REF}. The clock frequency of clkl is controlled by V_{ctrl}. When V_{LL} is higher than -10V, controlled voltage (V_{ctrl}) become higher and the frequency of clkl arise until V_{LL} = -10V. In contrast, when V_{LL} is lower than -10V, controlled voltage (V_{ctrl}) become lower and the frequency of clkl become slower until V_{LL} = -10V. The 4-phase clock generator provides the charge pump with the adaptive control signal. The phase shift clock generator can generate clkd_1, clkd_2, clkd_3 and clkd_4. When control signal V_{ctrlp} is logic 0, the clock waveforms of clkd_1, clkd_2, clkd_3 and clkd_4 depict as

Fig. 4.2 (a). Otherwise, when control signal V_{ctrlp} is logic 1, the clock waveforms of clkd_1, clkd_2, clkd_3 and clkd_4 depict as Fig. 4.2 (b). The same as the positive charge pump in chapter 3, the peak current from V_{DDH} can be reduced by the three phase shift clock waveform. Lower peak current from V_{DDH} may improve transient response of the dc regulator which provide V_{DDH} to charge pump.

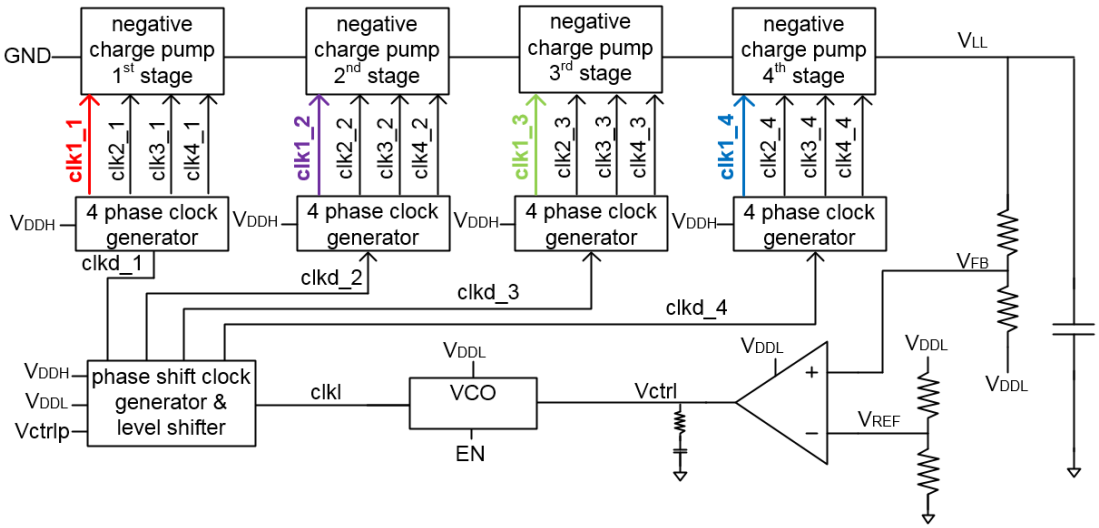
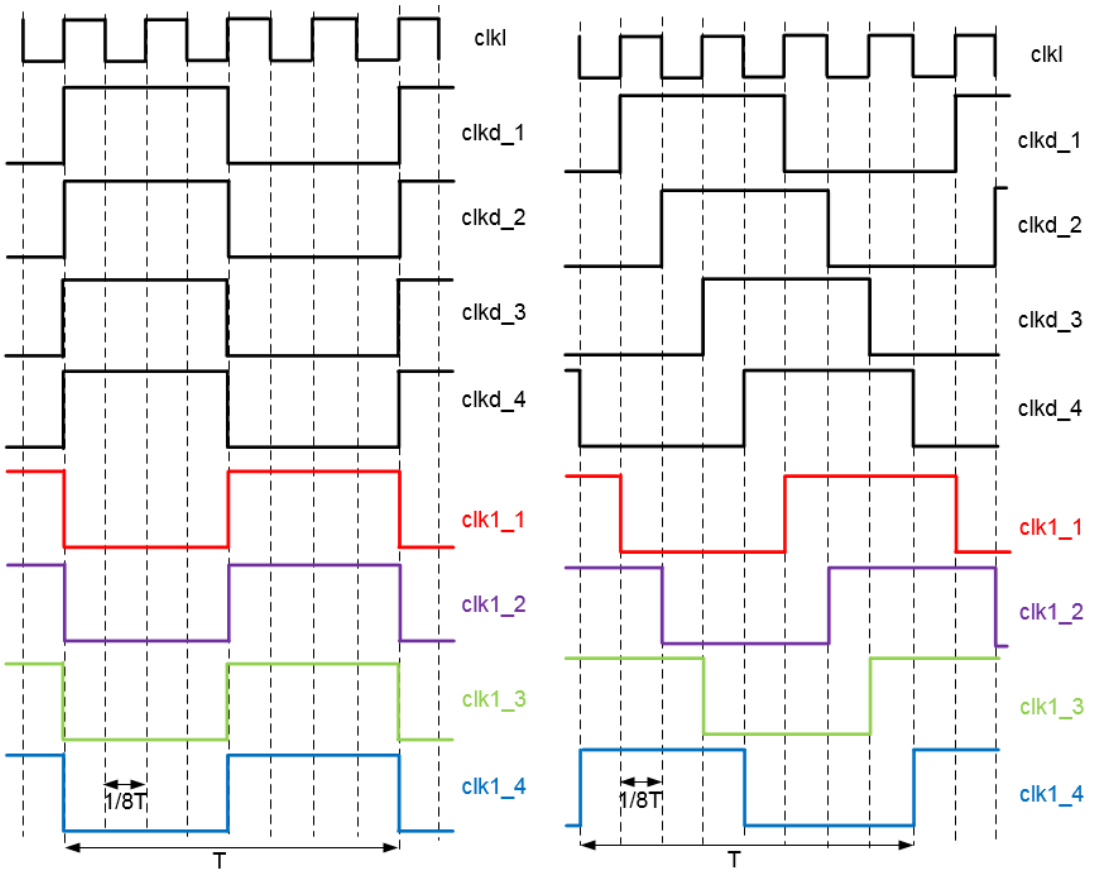


Fig. 4.1 Block diagram of negative charge pump.



(a) (b)

Fig. 4.2 (a)The clock waveform of clkd_1, clkd_2, clkd_3 and clkd_4 when V_{ctrlp} is low (0). (b) The clock waveform of clkd_1, clkd_2, clkd_3 and clkd_4 when V_{ctrlp} is high (1).

4.1.2 Negative Charge Pump and 4-phase Clock Generator

Fig. 4.3 shows the 4-phase cross couple negative charge pump circuit which is modified from [17]. The 4-phase cross-couple negative charge pump can reduce the output ripple and has no gate-oxide reliability issues. The negative charge pump consists of NMOS switches with deep N-Well which can isolate P-well of each NMOS from P-substrate. The bulk of each NMOS switch is connected to the source of NMOS. In this way, the NMOS switches don't have body effect and substrate leakage. All NMOS are 3.3V IO devices in 0.18-um 1.8-V/3.3-V CMOS process. Fig. 4.4 shows the

4-phase clock waveform (clk1, clk2, clk3 and clk4) and Fig. 4.5 shows the circuit of 4-phase clock generator.

Here, we separate 4-phase clock to eight intervals. At the interval t_1, the voltage of node 1 is GND and the voltage of node 2 is $-V_{DD}$. The voltage of node 3 is $V_{DD}-V_t$ and the voltage of node 4 is $-V_{DD}$, where V_{DD} is the voltage swing of clock and V_t is the threshold voltage of NMOS. Mb1, Mn2 and Mn3 are turned off and Mn1, Mb2 and Mn4 are turned on. The voltage of V_O become $-V_{DD}$ through Mn4.

At the interval t_2, the voltage of clk4 is dropped to low (GND). The voltage of node 3 is dropped to $-V_t$ to cut off Mn1. The voltage of node1, node 2 and node 4 are the same as the voltage at interval t_1. At the same time, Mb1, Mn2 and Mn3 keep being turned off and Mb2 and Mn4 keep being turned on.

At the interval t_3, the voltage of clk2 is dropped to low (GND). The voltage of node 1 is dropped to $-V_{DD}$ to turn on Mb1 and to turn off Mn4, and the voltage of node 3 is dropped to $-V_{DD}$ through Mb1. The voltage of node 2 and node 4 keep the same as the voltage at interval t_2. At the same time, Mn1, Mn2 and Mn3 keep being turned off and Mb2 keeps being turned on.

At the interval t_4, the voltage of clk1 is rose to high (V_{DD}). The voltage of node 2 is rose to GND to turn on Mn2 and to cut off Mb2, and the voltage of node 4 is rose to $-V_t$ as the voltage of node 2 was rose. The voltage of V_O become $-V_{DD}$ through Mn2, and the voltage of node 1 and node 3 are the same as the voltage at time interval t_3. Mn1 and Mn2 keep being turned off and Mb1 keep being turned on to cut off Mn1.

At the interval t_5, the voltage of clk3 is rose to high (V_{DD}). The voltage of node 4 is rose to $V_{DD}-V_t$ to turn on Mn3, and the voltage of node 2 is the same as GND. The voltage of node 1 and node 3 keep $-V_{DD}$. Mn1, Mb2 and Mn4 keep being turned off and Mb1 and Mn2 keep being turned on.

At the interval t_6, the voltage of clk3 is dropped to low (GND). The voltage of node 4 is dropped to $-V_t$ to cut off Mn3. The voltage of node1, node 2 and node 3 are the same as the voltage at time interval t_5. Mn1, Mb2 and Mn4 keep being turned off and Mb1 and Mn2 keep being turned on.

At the interval t_7, the voltage of clk1 is dropped to low (GND). The voltage of node 2 is dropped to $-V_{DD}$ to cut off Mn2 and to turn on Mb1, and the voltage of node 3 is dropped to $-V_{DD}$ as well. The voltage of node 2 and node 4 are the same as the voltage at time interval t_6. Mn1, Mn3 and Mn4 keep being turned off and Mb2 keep being turned on.

At the interval t_8, the voltage of clk2 is rose to high (V_{DD}) to turn on Mn4 and Mb1 is turned off at the same time. The voltage of node 3 is rose to $-V_t$. The voltage of V_O become $-V_{DD}$ through Mn4, and the voltage of node 2 and node 3 are the same as the voltage at time interval t_7. Mn1, Mn2 and Mn3 keep being turned off and Mb2 keep being turned on.

By these operations, the output voltage can be pumped to negative high voltage without body effect. Because the NMOS switches have been cut off before the voltage of node is changed, there is no return-back leakage current. Moreover, this negative charge pump can operate without gate-oxide reliability issues.

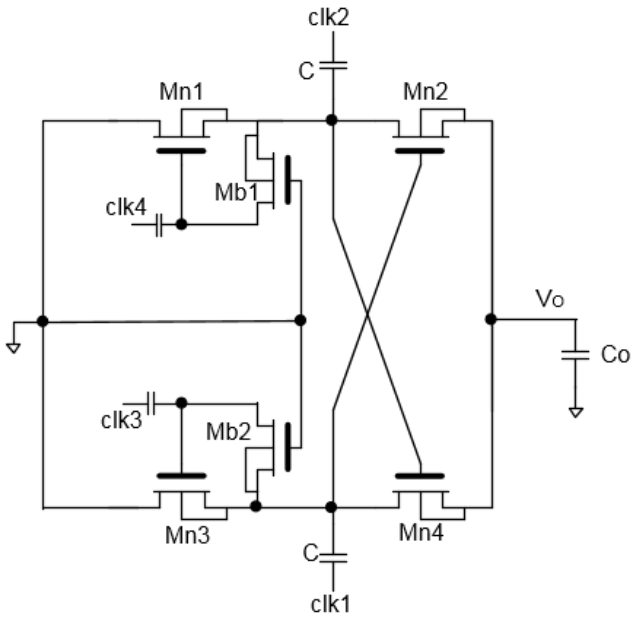


Fig. 4.3 One stage of proposed negative charge pump.

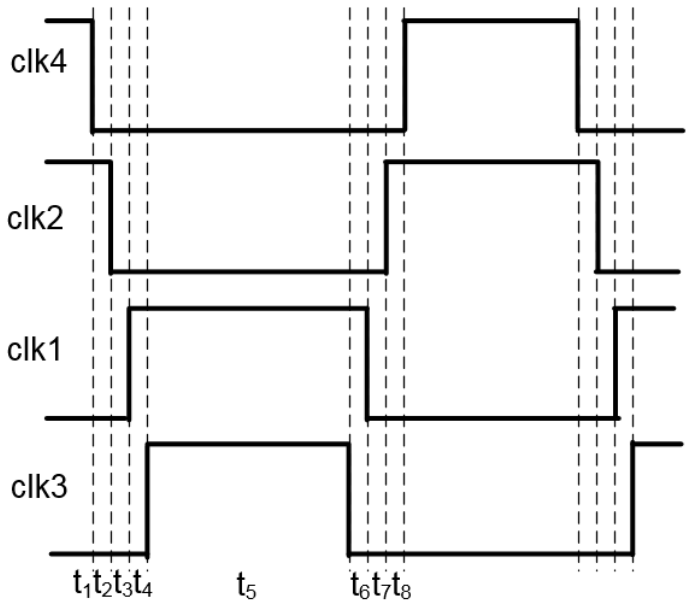


Fig. 4.4 4-phase clock waveforms of clk1, clk2, clk3 and clk4.

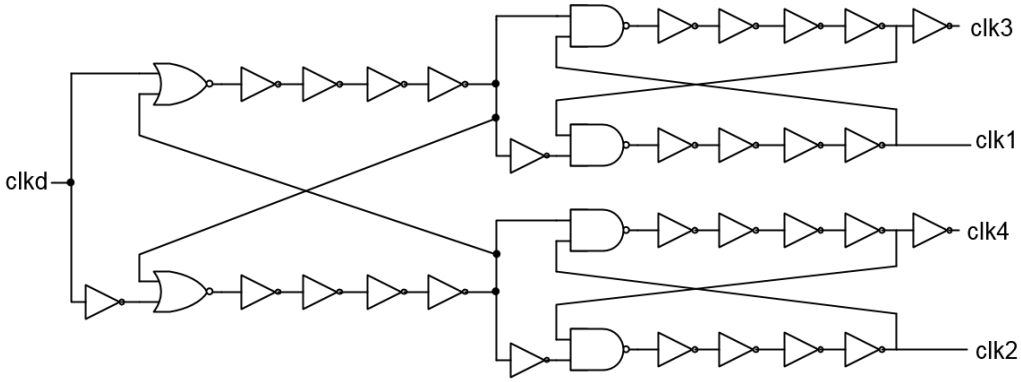


Fig. 4.5 4-phase clock generator.

Fig. 4.6 depicts the 4-stage cross-couple negative charge pump with some diodes which is used for start-up protection. When start-up, if both clk1_2 and clk3_2 are high, MN1 will be turned on and the voltage of node 2 will be equal to the voltage of V_{O1}. If the voltage of node 4 (V_4) is much higher the voltage of node 2 (V_2) which is express as Eq. (4-1), Mb2 will not be turned on all the time.

$$V_4 - V_{DD} - V_2 > V_{tn} \tag{4-1}$$

In this condition, the voltage of node 2 will be much lower and the voltage of node 4 will keep high after some clock cycles, which may cause overstress between node 2 and node 4 and damage the gate oxide of NMOS. So, we add some diode to discharge the node voltage during start-up. Fig. 4.7 depicts the connection of deep N-well in the charge pump circuit.

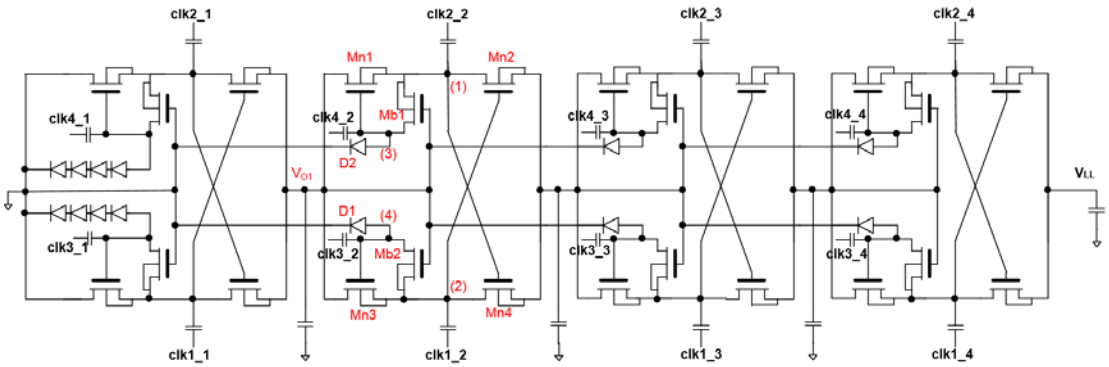


Fig. 4.6 4-stage cross couple negative charge pump.

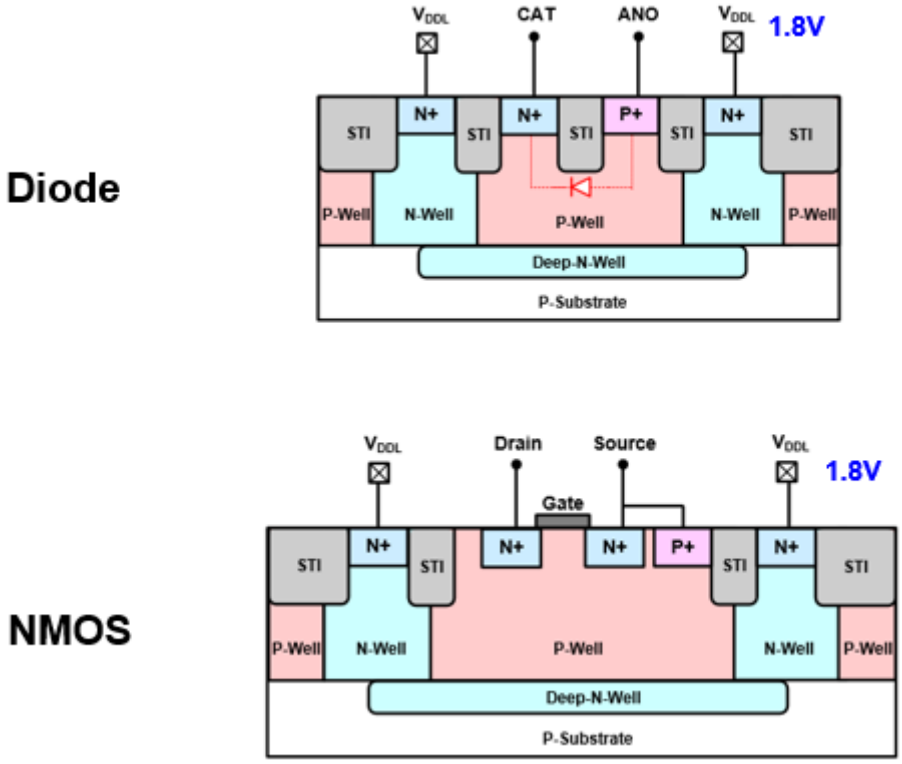


Fig. 4.7 Connection of deep N-well in the charge pump circuit.

4.1.3 Error Amplifier, VCO and Phase Shift Clock Generator

The error amplifier and VCO are the same as that are used in chapter 3. Fig. 4.8 shows the circuit diagram of phase shift clock generator, which consists of frequency divider, double edge trigger D flip-flop (DETFF), level shifter and some transmission gates. The frequency divider can divide frequency of clk by 4 and output clock to DETDFF. The transmission gates are used to control if the phase of clkd_1, clkd_2, clkd_3 and clkd_4 has phase shift different from each other. The level shifter can transfer 1.8V clock signal to 3.3V clock signal. When control signal V_{ctrlp} is logic 0, the output clock signals (clkd_1, clkd_2, clkd_3 and clkd_4) are the same phase like Fig. 4.2 (a). When control signal V_{ctrlp} is logic 1, the output clock signals (clkd_1, clkd_2, clkd_3 and clkd_4) have phase shift like Fig. 4.2 (b).

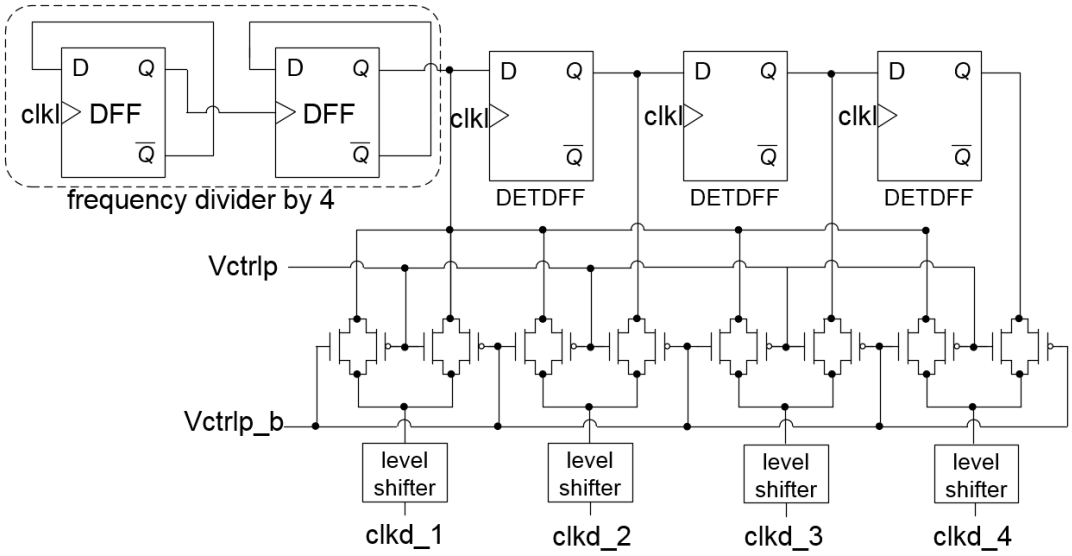
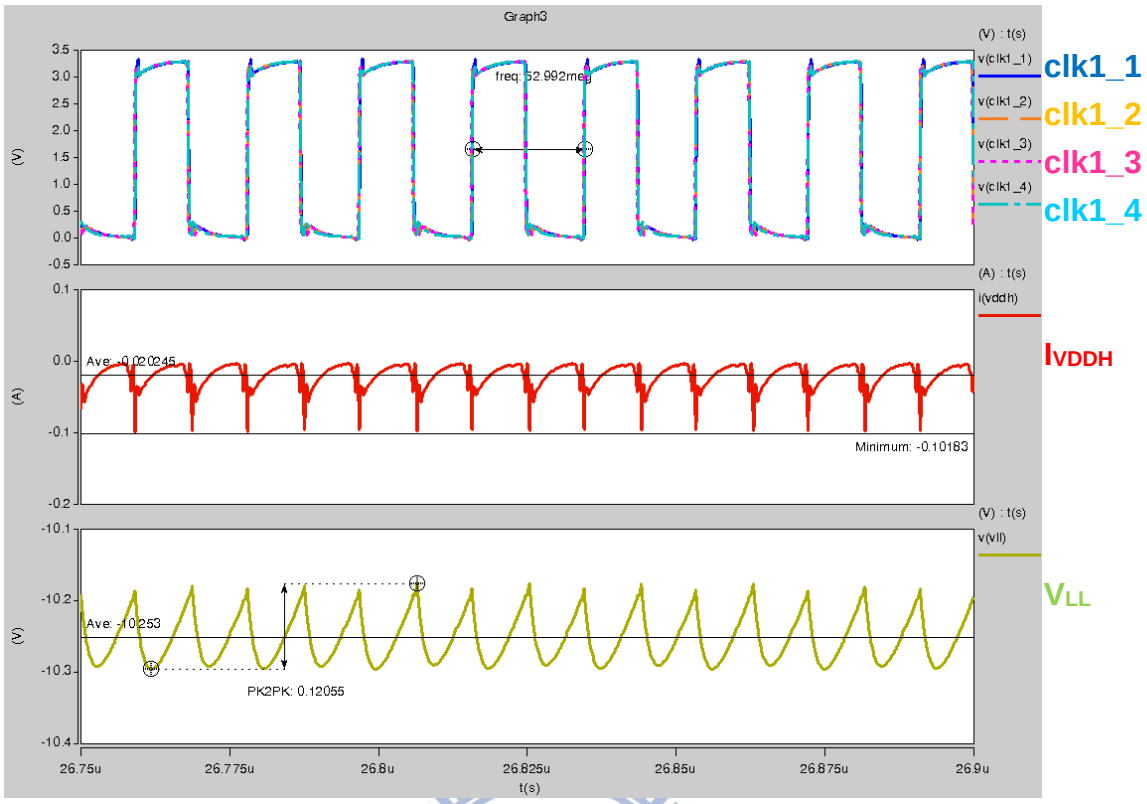


Fig. 4.8 Circuit of phase shift clock generator.

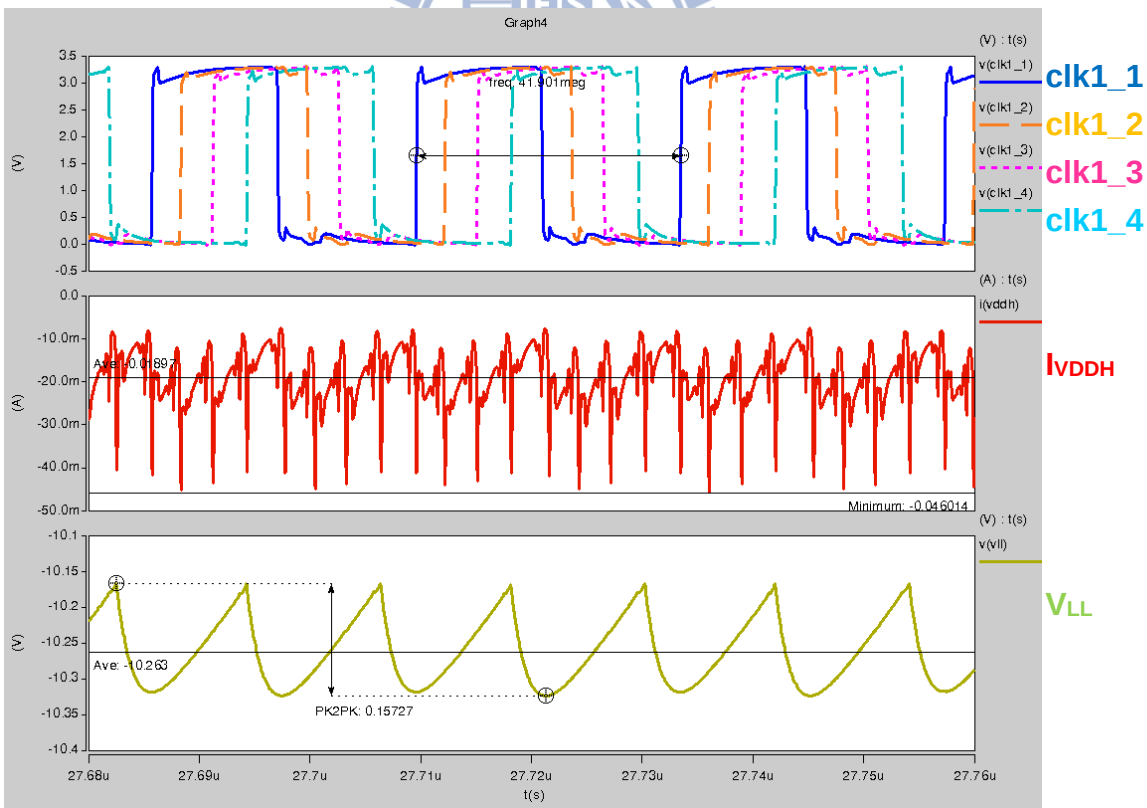
4.2 Simulation Results

This work have been simulated in HSPICE with TSMC 0.18-μm 1.8-V/3.3-V CMOS process. Fig. 4.9 (a) depicts the simulation result of charge pump when V_{ctrlp}=0 and I_{load}=3.5mA. The clock signals (clk_1, clk_2, clk1_3, and clk1_4) charge pump don't have phase shift. The pumping frequency is 53MHz. The input peak current ($I_{VDDH(max)}$) is 101.83mA and the average output voltage (V_{CC}) is about -10.253V. The efficiency of charge pump is 53.31%.

Fig. 4.9 (b) depicts the simulation result of charge pump when V_{ctrlp}=1 and I_{load}=3.5mA. The clock signals (clk_1, clk_2, clk1_3, and clk1_4) charge pump have phase shift. The pumping frequency is 41.9MHz. The input peak current ($I_{VDDH(max)}$) is 46mA and the average output voltage (V_{CC}) is about -10.263V. The efficiency of charge pump is 54.15%. As the simulation result, we can reduce the input peak current with phase shift clock control.



(a)



(b)

Fig. 4.9 Simulation result of charge pump when (a)V_{ctrlp}=0 and I_{load}=3.5mA (b)V_{ctrlp}=1 and I_{load}=3.5mA.

4.3 Measurement Results

This work have been simulated by HSPICE and have been fabricated in TSMC 0.18-μm 1.8-V/3.3-V CMOS process. The charge pump aims to output voltage about -10V and maximum current 3.5mA. The pumping capacitors of charge pump are 50pF and the output capacitor is 100pF. All capacitors of the negative charge pump are fully on-chip. Fig. 4.10 depicts the die photo of test chip, which includes the 4-stage charge pump and 4-phase clock generator (A), output capacitor of charge pump (B), and VCO, error amplifier and phase shift clock generator (C). The test chip area is 2.45 x 1.48mm^2.

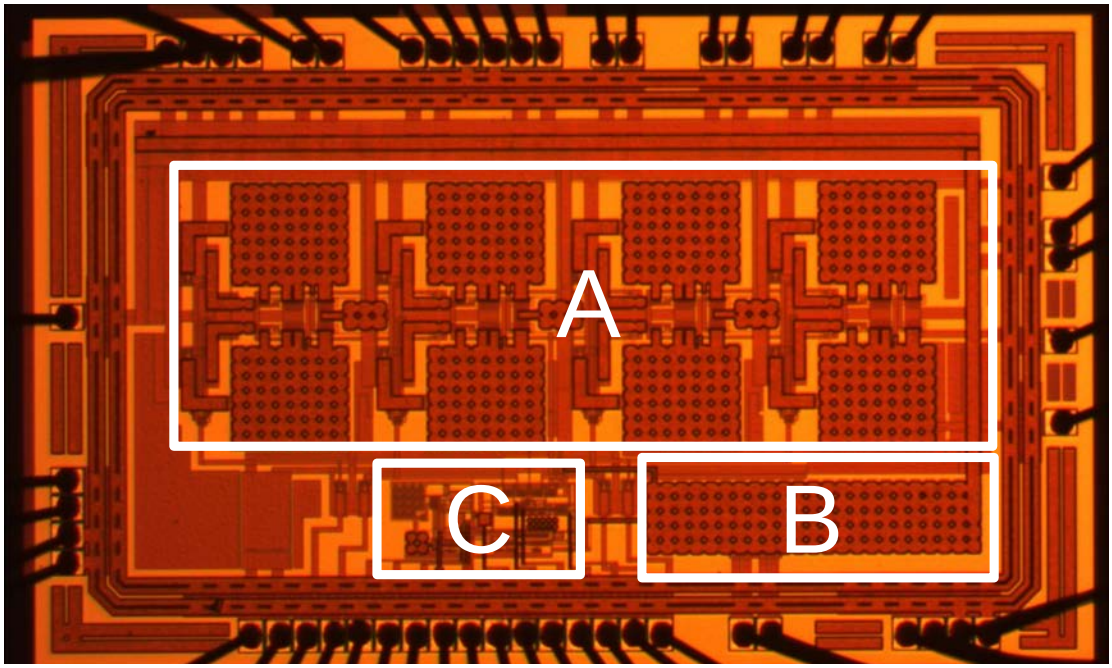


Fig. 4.10 Die photograph with A: 4-stage charge pump and 4-phase clock generator, B: output capacitor of charge pump, and C: VCO, error amplifier and phase shift clock generator.

Fig. 4.11 depicts the measurement setup of test chip. The same as the measurement setup of the positive charge pump, Agilent B2902A is used to provide voltage 1.8V V_{DDL} and 3.25V V_{DDH}, which is also used to measurement power consumption of the

charge pump. Tektronix MSO 5104 is used to observe the waveforms of the charge pump.

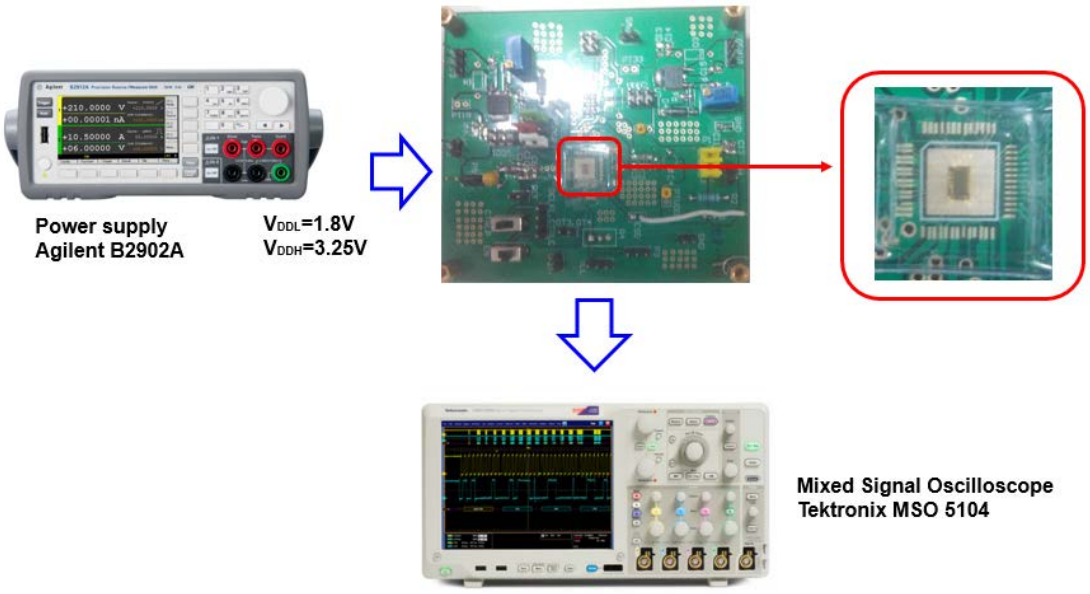


Fig. 4.11 Measurement setup of test chip.

Fig. 4.12 depicts the measurement result of power on time at I_{load} is 3.5mA and V_{ctrlp} is logic 1, which is about 962nsec. Fig. 4.13 depicts the waveforms to check the phase shift clock generator function. V_{ctrlp} =0 means the clock signal of each stage doesn't have phase shift. V_{ctrlp} =1 means the clock signals of each stage has phase shift. The signals OT1, OT2, OT3 and OT4 are generated by clkd_1, clkd_2, clkd_3 and clkd_4 via some buffers respectively. As the measurement result, the function of phase shift clock generator is working.

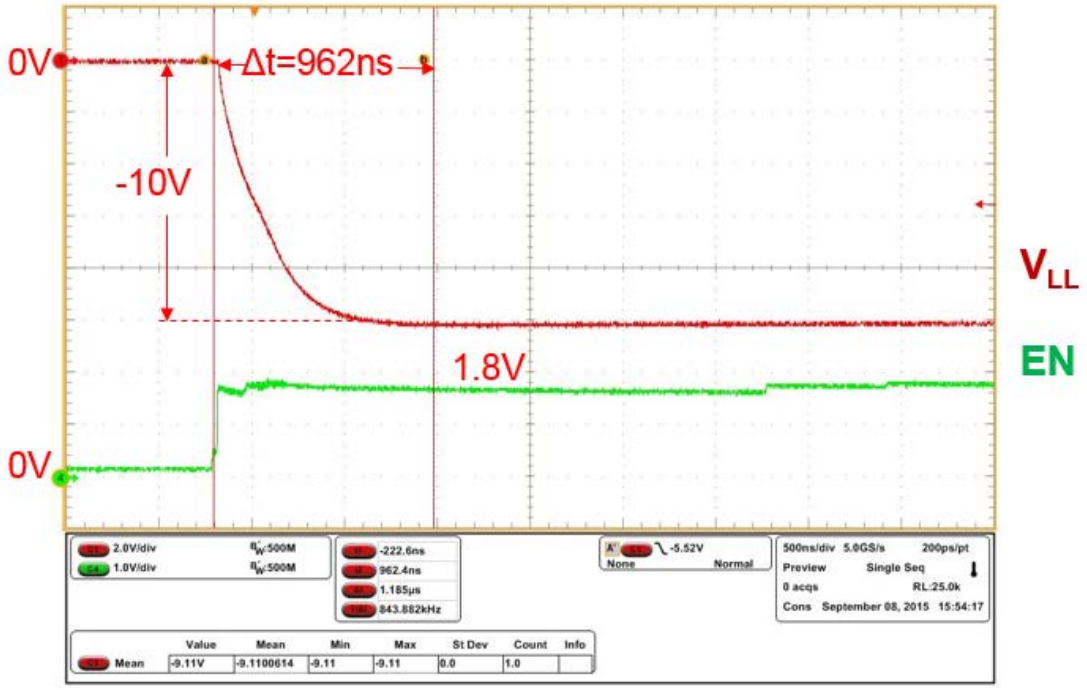


Fig. 4.12 Measurement of power on time.

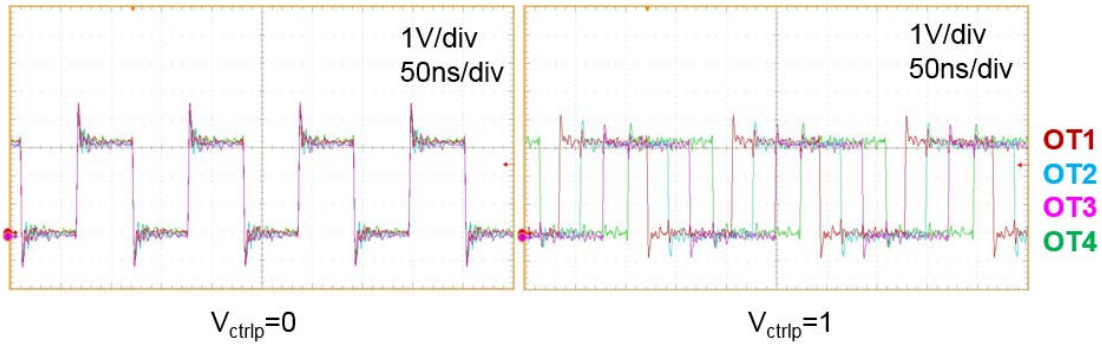


Fig. 4.13 Measurement of phase shift clock generator.

Fig. 4.14 depicts the measurement result of V_{LL} when I_{load} is 3.5mA. The efficiency is calculated by Eq. (4.2), where P_{VLL} is the power of V_{LL}.

$$\text{Efficiency} = \frac{P_{VLL}}{P_{VDDH}+P_{VDDL}} \tag{4.2}$$

When V_{ctrlp} is logic low (GND), the average voltage of V_{LL} is -9.745V, the ripple of V_{LL} is 141.87mV, and the efficiency is 50.64%. When V_{ctrlp} is logic high (V_{DDL}), the average voltage of V_{LL} is -10.272V, the ripple of V_{LL} is 141.87mV, and the efficiency is 46.82%. Fig. 4.15 show the measurement result of output voltage (V_{LL}) versus

different loading current (I_{load}). Fig. 4.16 show the measurement result of efficiency versus different loading current (I_{load}). Fig. 4.17 show the measurement result of output ripple versus different loading current (I_{load}).

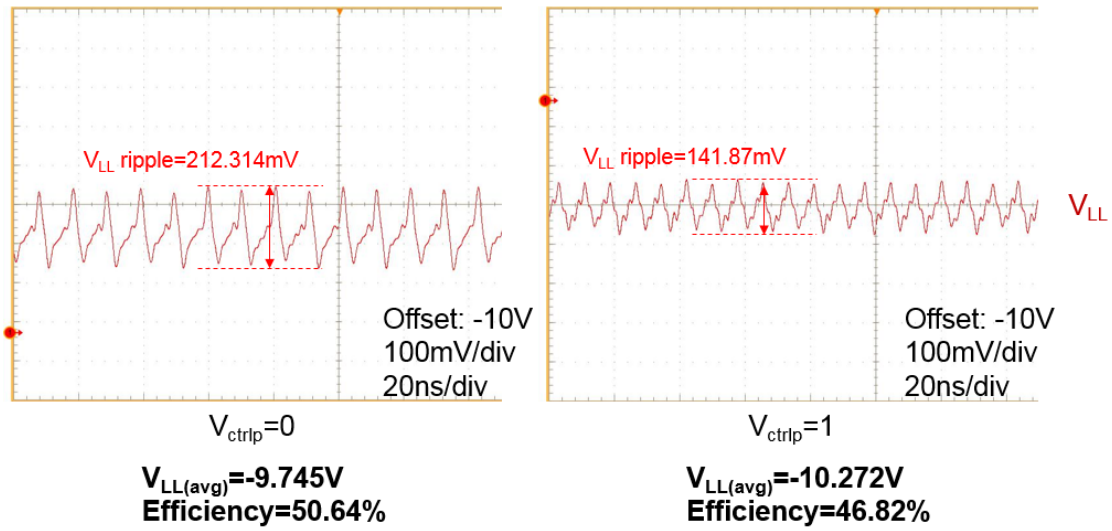


Fig. 4.14 Measurement of V_{LL} when I_{load} is 3.5mA.

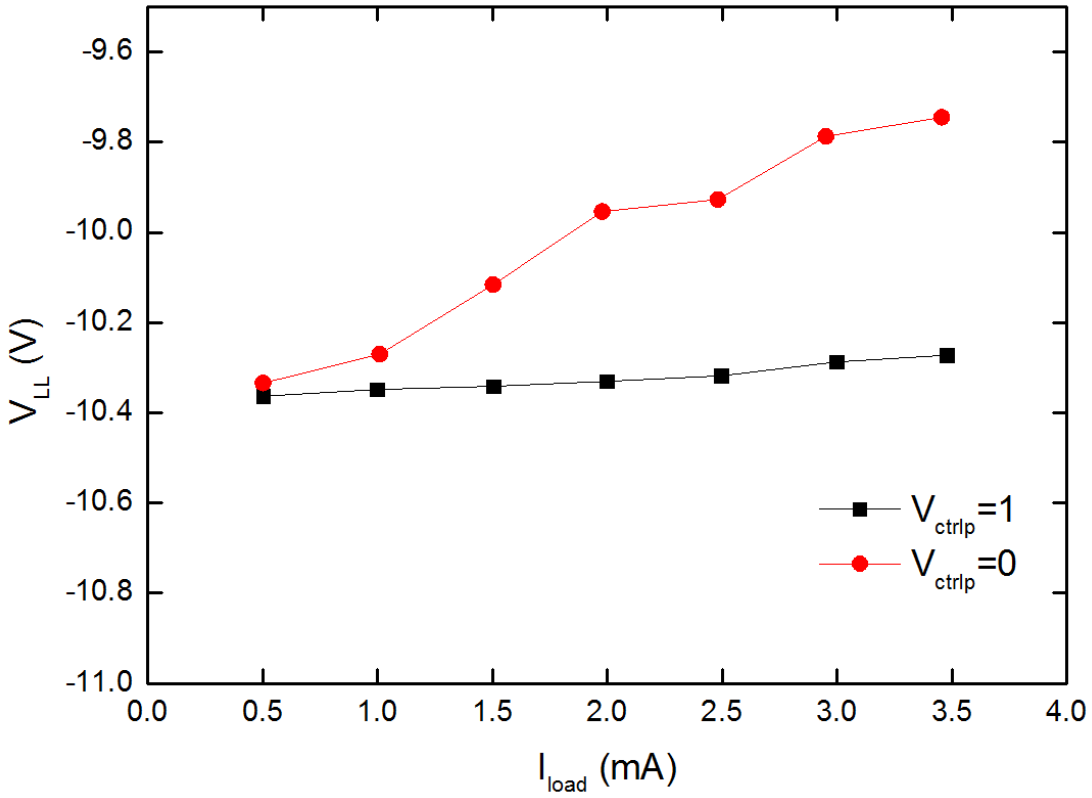


Fig. 4.15 Measurement of output voltage (V_{LL}) versus different loading current (I_{load}).

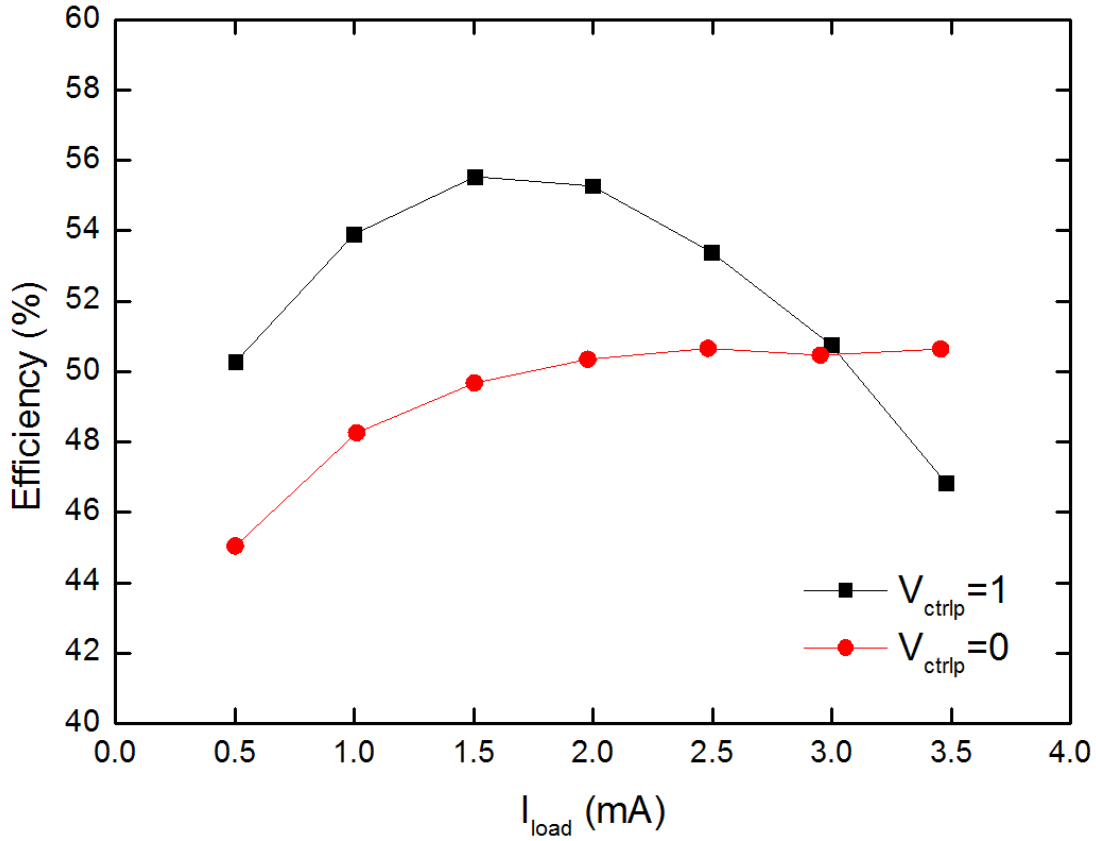


Fig. 4.16 Measurement of efficiency versus different loading current (I_{load}).

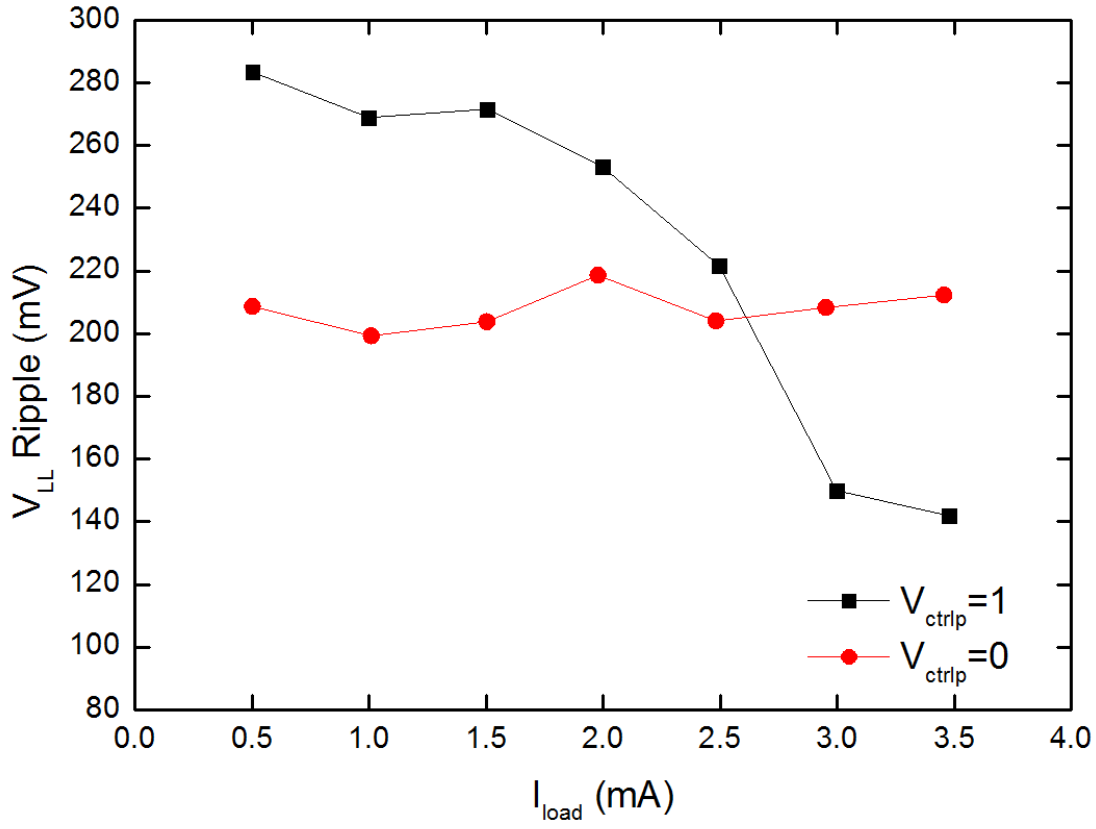


Fig. 4.17 Measurement of output ripple versus different loading current (I_{load}).

In order to measurement input peak current ($I_{VDDH(max)}$) from V_{DDH}, we add a 5Ω resistance between node V_{DDH2} and V_{DDH} and measure the voltage difference between V_{DDH2} and V_{DDH}. Fig 4.18 shows the measurement setup. Fig. 4.19 depicts the measurement result of input current (I_{VDDH}) from V_{DDH} when I_{load} is 1.5mA. When V_{ctrlp} is logic low (GND), the maximum input peak current ($I_{VDDH(max)}$) is 59.25mA. When V_{ctrlp} is logic high (V_{DDL}), the maximum input peak current ($I_{VDDH(max)}$) is 29.3mA.

Fig. 4.20 depicts the measurement result of input current (I_{VDDH}) from V_{DDH} when I_{load} is 3.2mA. When V_{ctrlp} is logic low (GND), the maximum input peak current ($I_{VDDH(max)}$) is 44.28mA. When V_{ctrlp} is logic high (V_{DDL}), the maximum input peak current ($I_{VDDH(max)}$) is 39.23mA. Fig. 4.21 shows the measurement result of $I_{VDDH(max)}$ versus different loading current in three different chip. In the measurement result, the maximum input peak current can be reduce by applying phase shift clock (clkd_1, clkd_2, clkd_3 and clkd_4) to the charge pump. Table 4.1 is the comparison of post-simulation and measurement.

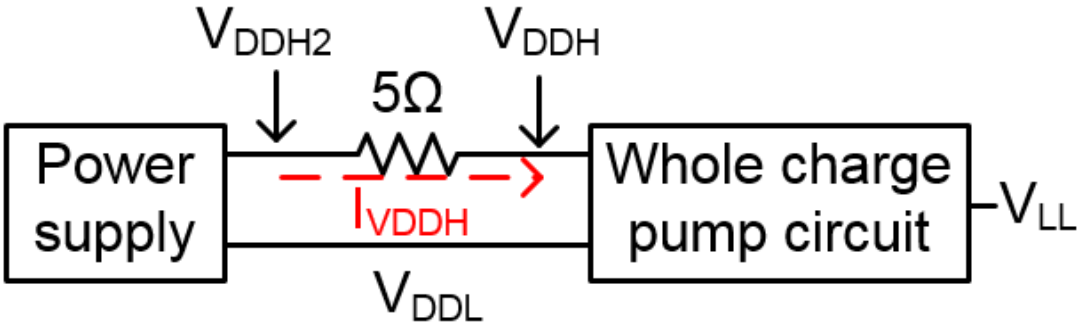


Fig. 4.18 The measurement setup for measuring I_{VDDH}.

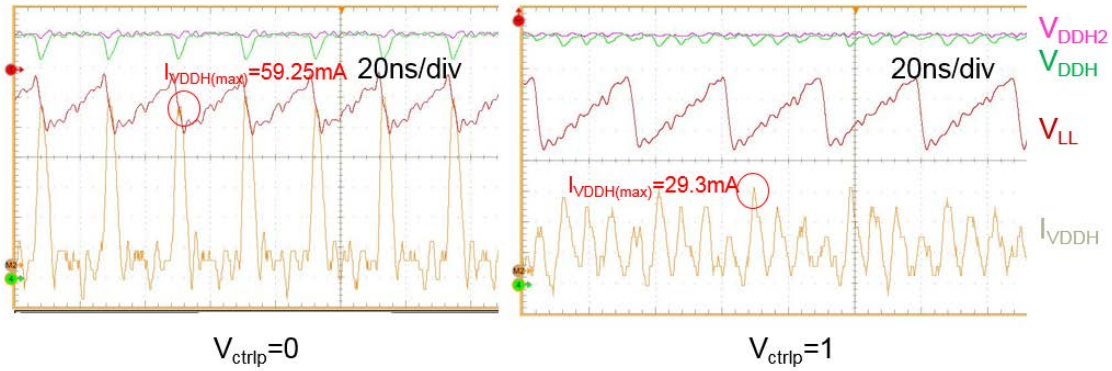


Fig. 4.19 The measurement result of input current (I_{VDDH}) from V_{DDH} when I_{load} is 1.5mA.

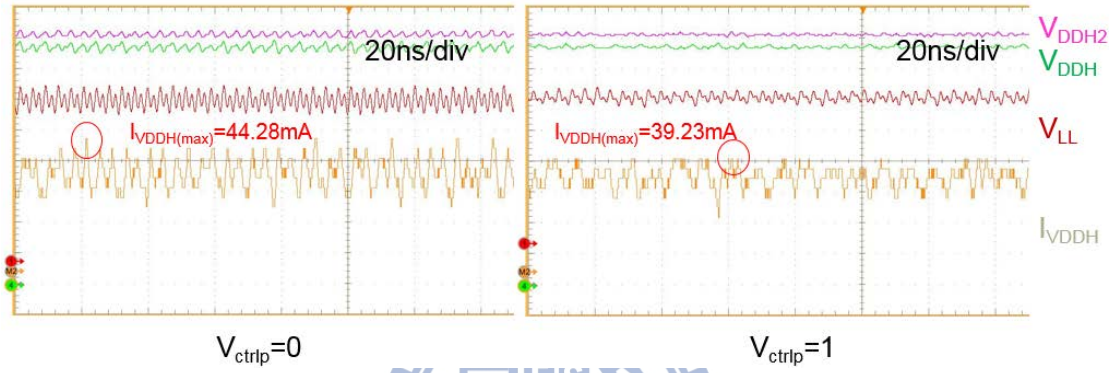


Fig. 4.20 The measurement result of input current (I_{VDDH}) from V_{DDH} when I_{load} is 3.2mA.

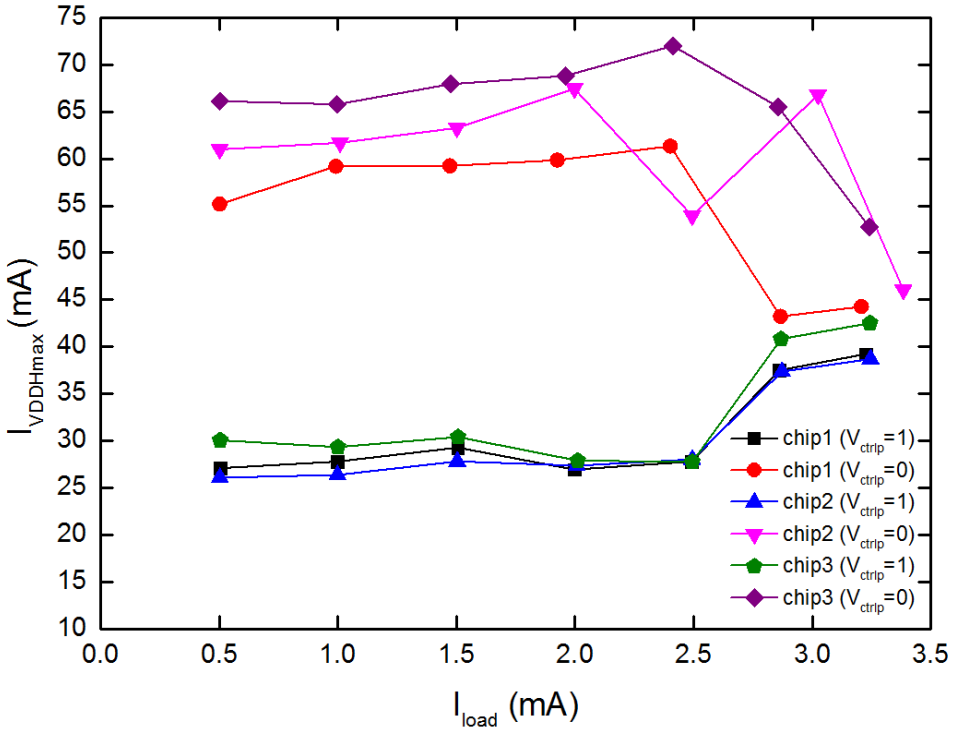


Fig. 4.21 The measurement result of $I_{VDDHmax}$ versus different loading current in three different chip.

Table. 4.1 Comparison of post-simulation and measurement.

		Post-layout simulation (TT)	Measurement
Power supply V_{DDL} / V_{DDH}		1.8V / 3.25V	1.8V / 3.25V
$I_{VDDHmax}$ V_{ctrlp} = 0 / V_{ctrlp} = 1		101.83mA / 46mA (I_{load}=3.5mA)	44.28mA / 39.23mA (I_{load}=3.2mA)
V_{CC} / Efficiency (V_{ctrlp} = 1)	0.5mA	-10.31V / 57.208%	-10.363V / 50.27%
	1mA	-10.297V / 59.45%	-10.348V / 53.9%
	1.5mA	-10.293V / 60.06%	-10.341V / 55.54%
	2mA	-10.283V / 60.05%	-10.33V / 55.27%
	2.5mA	-10.278V / 59.56%	-10.31V / 53.39%
	3mA	-10.272V / 58.68%	-10.287V / 50.75%
	3.5mA	-10.263V / 57.15%	-10.272V / 46.82%
Process		TSMC 0.18μm 1.8V/3.3V CMOS Process	

Fig. 4.22 depicts the transient response of a regulator. Theoretically, the lower peak loading current, the better transient response the regulator has. In this work, in order to observe the influence of lower peak current, we use a commercial dc-dc converter LM317 instead of power supply to supply 3.25V (V_{DDH}). The measurement setup is shown as Fig. 4.23. We use LM317 to generate V_{DDH} (3.25V) instead of using power supply. Fig. 4.24 depicts the measurement environment. Fig. 4.25 depicts the circuit diagram of LM317. The charge pump and LM317 are on the same PCB broad, and we probe the output voltage (V_{DDH}) of LM317 to observe the waveform.

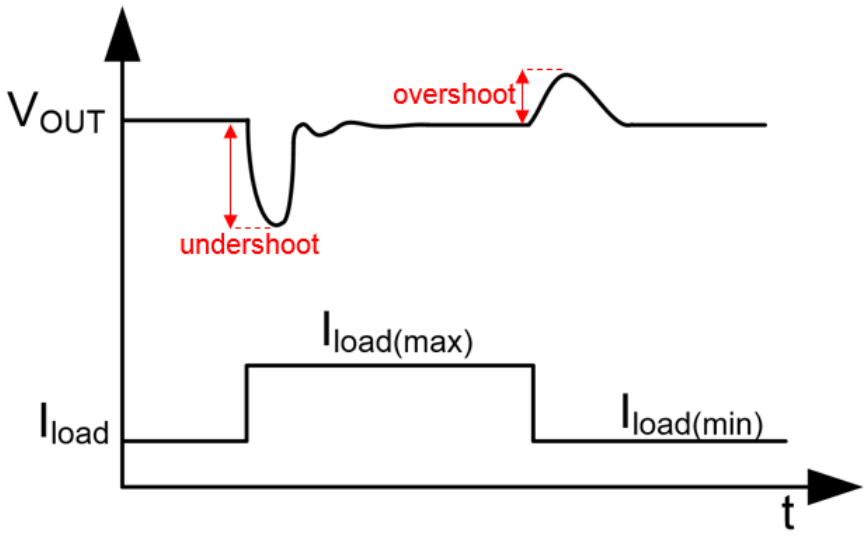


Fig. 4.22 Transient response of regulator.

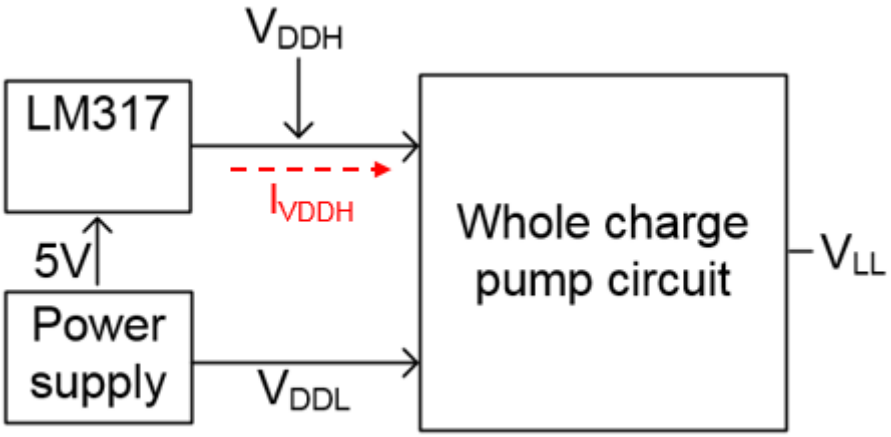


Fig. 4.23 The measurement setup to observe the influence of lower peak current.

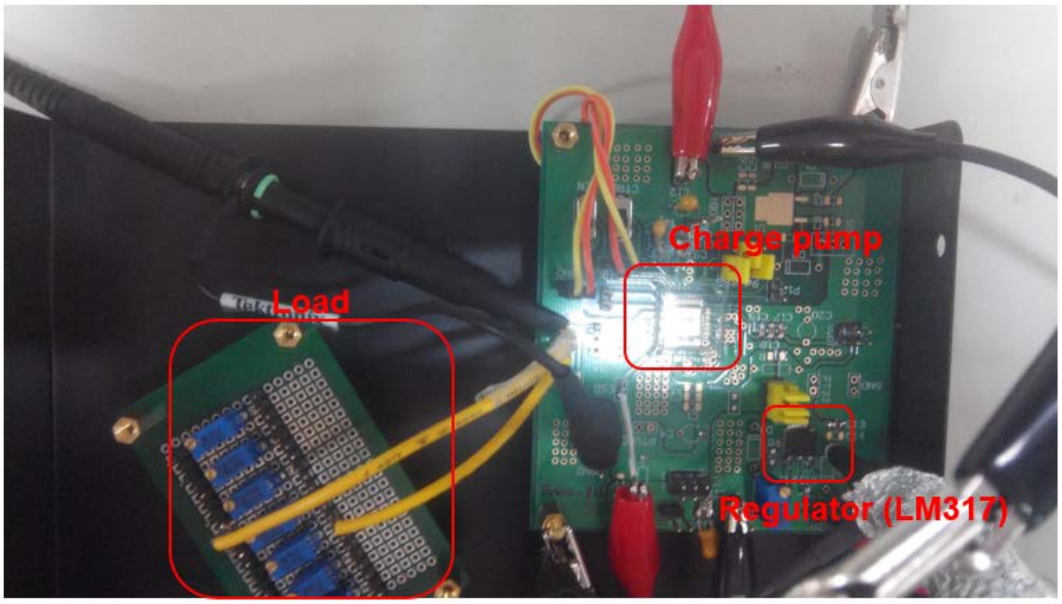


Fig. 4.24 The measurement environment to observe output voltage of LM317.

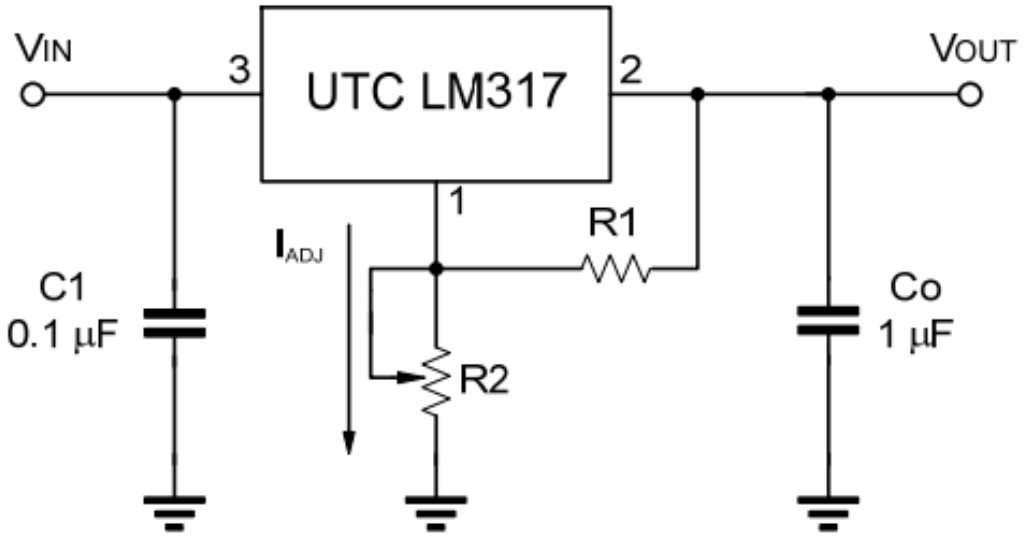


Fig. 4.25 The circuit diagram of LM317.

Fig. 4.26 depicts the waveform of V_{DDH} which is generated by LM317 when charge pump is turned off. The average voltage is 3.246V. Fig. 4.27 depicts the waveforms of V_{DDH} in different control voltage. When V_{ctrlp} is logic low (GND), the overshoot voltage of V_{DDH} is 3.337V and the undershoot voltage of V_{DDH} is 3.151V. When V_{ctrlp} is logic high (V_{DDL}), the overshoot voltage of V_{DDH} is 3.271V and the undershoot voltage of V_{DDH} is 3.222V. By the measurement result, we can observe that the lower input current of V_{DDH} can enhance the transient response of LM317.

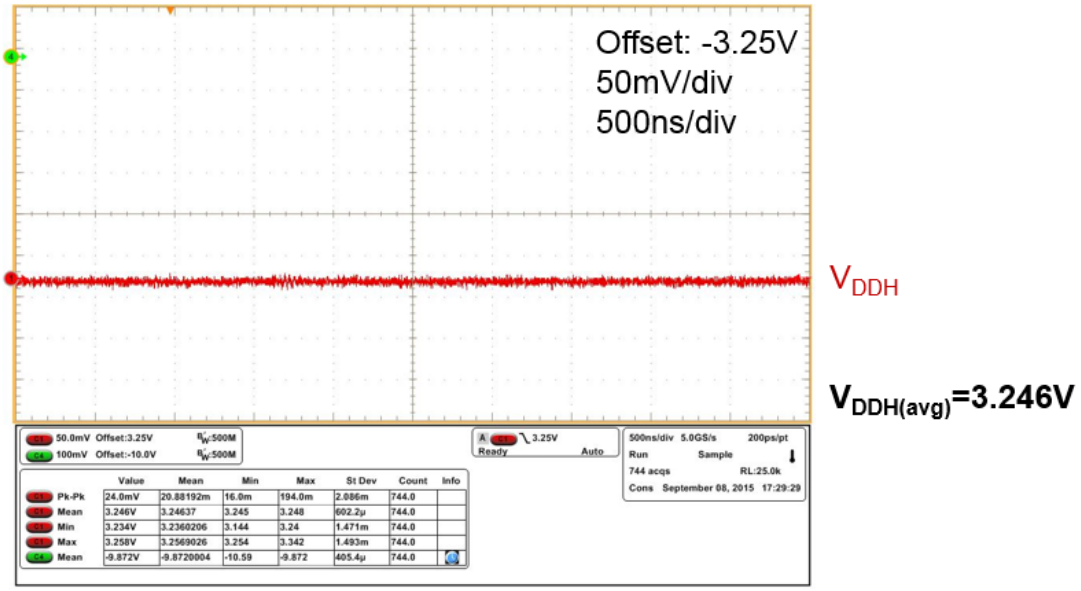


Fig. 4.26 The waveform of V_{DDH} when charge pump is turned off.

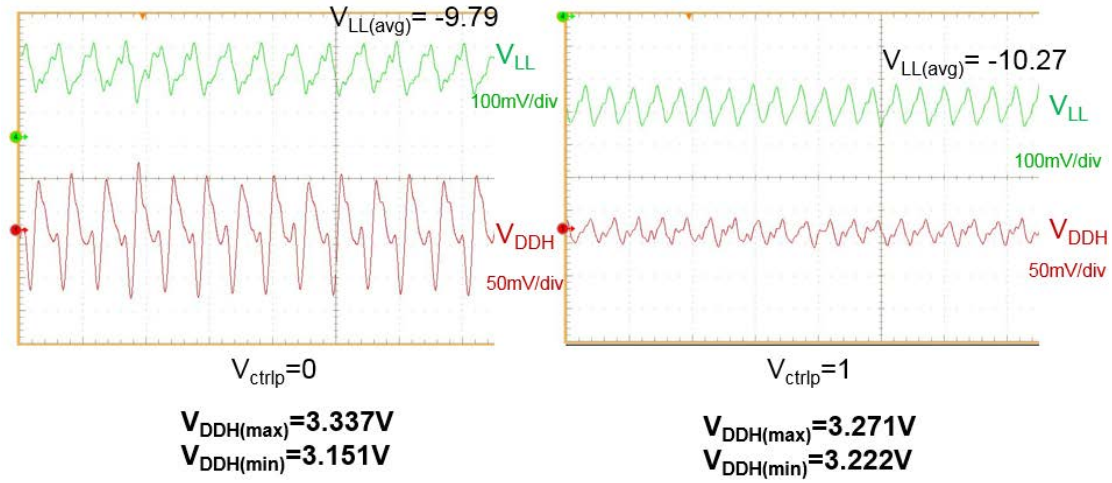


Fig. 4.27 The waveform of V_{DDH} in different control voltage (V_{ctrlp}).

Moreover, we measure the leakage current of MIM capacitor in TSMC 0.18μm 1.8-V/3.3-V CMOS process by Agilent B1505A. Fig.4.28 depicts the measurement result. The capacitor is 25pF and the effective area is 22500μm^2. When the voltage difference across MIM capacitor reach about 31V, the leakage current is 1nA. In this work, the maximum voltage difference across MIM capacitor is about 10V~12V, and the leakage current is about 100pA. By this measurement, the MIM capacitor would not breakdown during circuit operation of charge pumps.

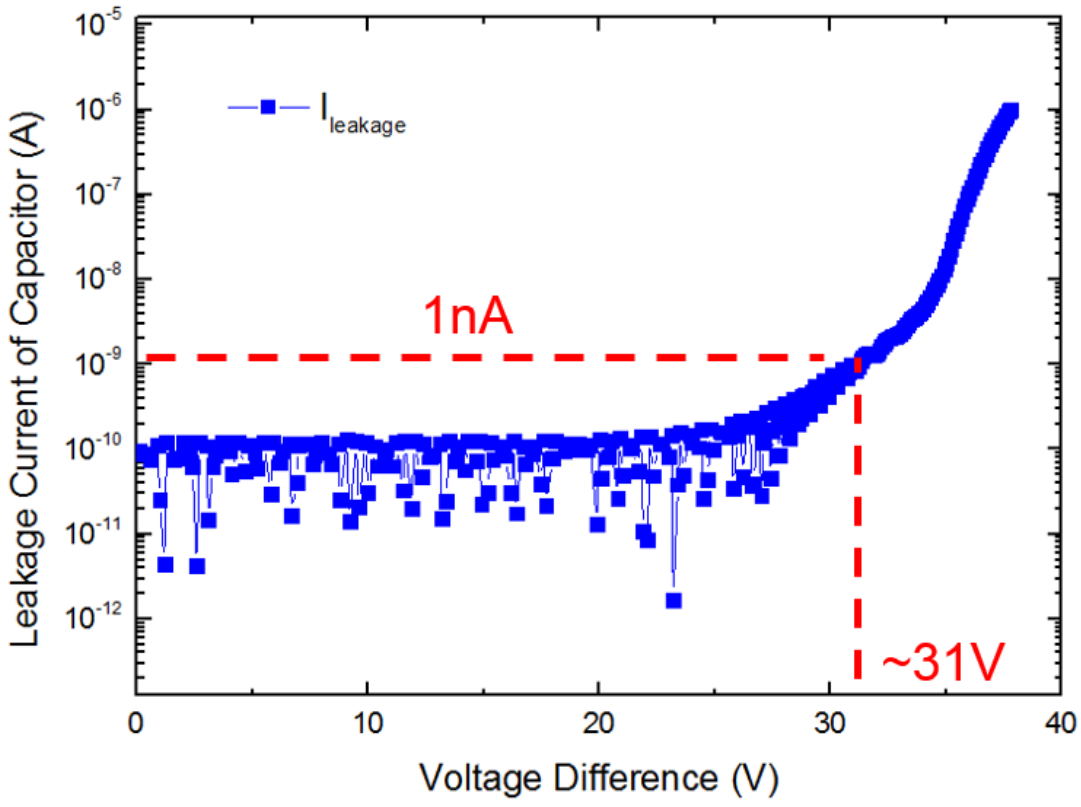


Fig. 4.28 The measurement result of MIM capacitor.

4.4 Summary

Design of a negative charge pump regulator for biomedical implant is investigated and verified in this chapter. The circuit design have been fabricated in TSMC 0.18-μm 1.8-V/3.3V CMOS process. The proposed design can output about -10.3V high voltage and maximum output current 3.5mA without the issues of electrical overstress and gate-oxide reliability. The 4-phase cross-couple negative charge pump is used. Each stage of charge pump has its own clock signal which has phase shift different from each other. By the measurement, the clock control scheme can reduce the maximum peak current which flow from power supply V_{DDH}, and we also used a dc-dc converter LM317 to test this function.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

5.1.1 Positive Charge Pump

The positive charge pump can generate high voltage which is about 10.8V, and can output 3.5mA maximum loading current without gate-oxide reliability issues. By the phase shift clock control scheme, this circuit can reduce the maximum peak input current. This circuit is fabricated in TSMC 0.18μm 1.8-V/3.3-V CMOS process and die area is 1.87 x 1.48mm^2. All charge pump circuit are realized fully on chip. The charge pump also had been fabricated in SoC for cochlear stimulation and could generate high voltage to stimulus driver.

5.1.2 Negative Cross-Couple Charge Pump

A negative cross-couple charge pump has been proposed and fabricated in TSMC 0.18μm 1.8-V/3.3-V CMOS process. All circuit are realize fully on chip, and die area is 2.45 x 1.48mm^2. The proposed design can generate negative high which is about -10.3V, and can output 3.5mA maximum loading current. This circuit can operate without gate-oxide reliability issues and return-back leakage current. We also used LM317 to observe the effect of peak loading current, and the transient response can be enhance by the lower peak loading current. Moreover, we measure the leakage of MIM capacitor to check the reliability of this charge pump circuit.

5.2 Future Works

5.2.1 Charge Sharing

Some methods to enhance the efficiency of charge had been proposed, such as charge sharing concept [18]~[21]. By recycling wasted charges in clock buffers of charge pump, the power consumption of charge pump can be reduce. Fig. 5.1 depicts the charge sharing concept. In Fig 5.1 (a), the charges on parasitic capacitance C_{PBB} are

dumped to ground and wasted. In charge sharing clock scheme, there is an intermediate voltage level before clock buffer outputs, some charges on C_{PBB} can be stored on C_{PBA} before the charges on C_{PBB} are dumped as shown in Fig. 5.1 (b). Then, the voltage on C_{PBA} is charged to V_{DD} and the voltage on C_{PBB} is discharged to GND as shown in Fig. 5.1 (c). By this method, the voltage swing of the buffer output which is charge by the current from the power supply become half, and can reduce the loss of charge pump.

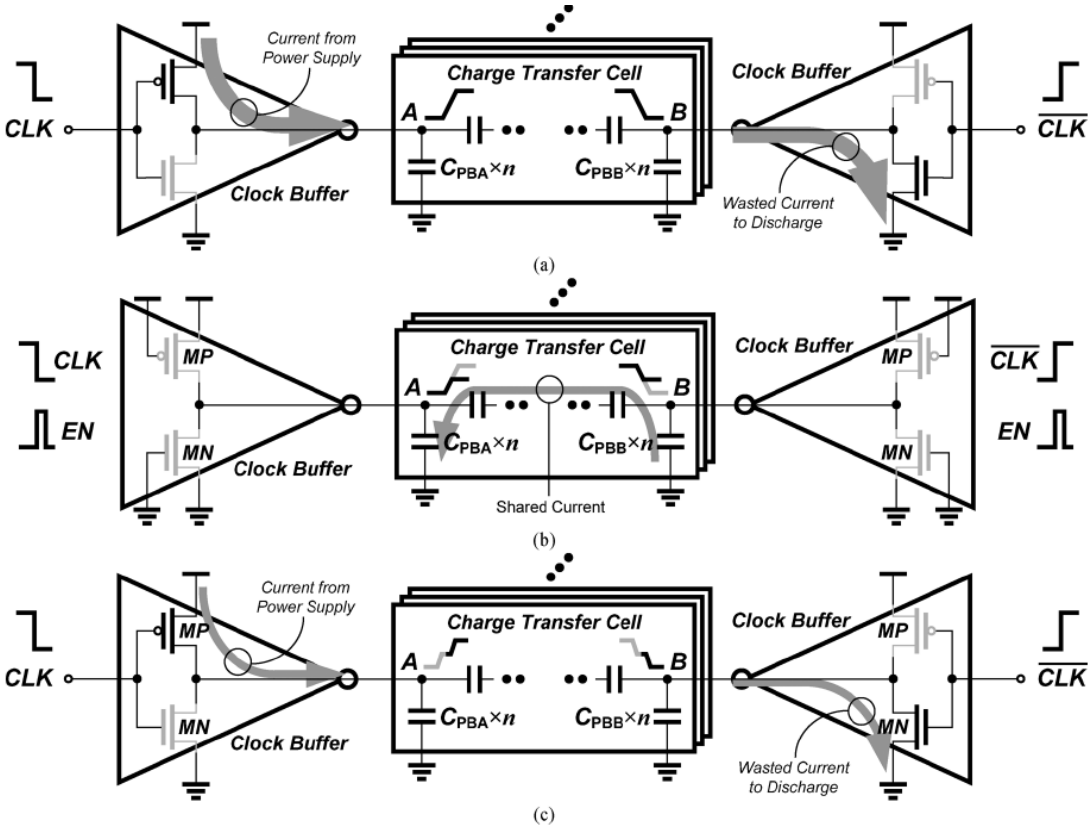


Fig. 5.1 The charge sharing concept [20].

5.2.2 Negative Charge Pump

Fig. 5.2 depicts the circuit of negative charge pump. As the circuit operation in charter 4, the maximum voltage of node 3 and node 4 are V_{DDH}-V_t, where the voltage drop (V_t) is cause by Mb1 and Mb2. When Mn1 or Mn3 is tuned on, the V_{GS} of the MOS switch is V_{DDH}-2V_t. This would cause more conduction loss on MOS switches and degrade the efficiency of charge pump. This problem need to be solve in the future.

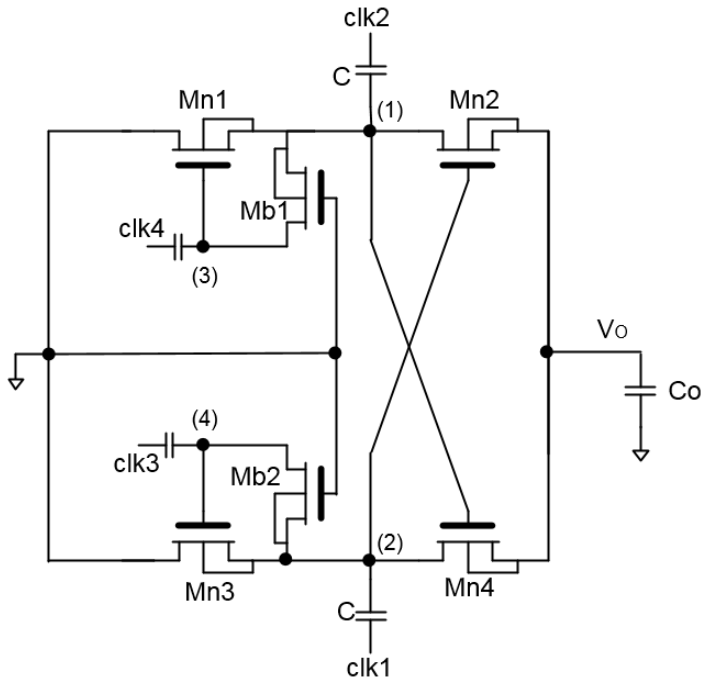


Fig. 5.2 The circuit of negative charge pump.

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