國立交通大學

電子研究所

碩　士　論　文

系統層級暫態干擾之靜電放電暫態偵測電路與湧浪數位轉換器之設計

Design of ESD Transient Detection Circuit and Surge-to-Digital Converter for Microelectronic Systems against Electrical Transient Disturbances

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指導教授: 柯明道教授 (Prof. Ming-Dou Ker)

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摘要

為了達到更高速與低功率消耗的電路應用，並且實現集合複雜功能的積體電路 (Integrated Circuits, ICs)，互補式金屬半導體積體電路製程尺寸日益微縮。在此改變下，積體電路對於靜電與湧浪造成的電磁干擾或是過度電性應力這類的可靠度議題在近日已變得不容忽視。無論在元件層級上，容易過壓或過電流的電晶體；系統層級中，低的電源電壓造成低的邏輯轉態電壓域值，像是從 3.3 伏特降至 1.8 伏特或甚至更低，這些皆會降積體電路對電磁干擾 (Electromagnetic Interference, EMI) 的免疫能力。因此系統層級靜電放電事件(System-Level ESD Events) 與湧浪事件(Surge Events) 防護變得尤為重要。

針對終端用戶的系統層級靜電放電事件與湧浪事件防護，有相對應的靜電放電規範 IEC 61000-4-2，與湧浪事件規範 IEC61000-4-5。由靜電放電電壓或湧浪的過電壓與電流引起的快速暫態雜訊會隨機耦合到為電子產品的電源線、輸入/輸出腳位上，進而引發產品不正常工作甚至是被損壞。為了增加系統的穩定性並

且能夠整合於積體電路內部，本論文分別提出一個晶片上暫態偵測電路以及一個晶片上的湧浪數位轉換器。

整合於積體電路內部的暫態偵測電路結合韌體程式設定的靜電放電防護法，已經被證明能夠有效提升微電子產品在系統層級靜電放電測試下的防護能力。本論文提出的暫態偵測電路採用無電阻與電容設計，經由 0.18-μm CMOS 製程技術實現。透過模擬及實際量測，提出之暫態偵測電路能夠成功偵測系統層級靜電放電所引起的電源擾動。處理器依據暫態電路之偵測結果判定系統是否受系統層級靜電放電威脅，並判定執行系統回復程序與否以達到產品對系統層級靜電放電反應要求之標準。

另外，本論文提出之湧浪數位轉換器經由 0.18-μm CMOS 製程技術實現。透過適當的模擬與量測，證明其能夠應用於晶片內湧浪防護去抵抗感應電壓所造成的湧浪或是經由電路板上的防護後所殘餘的電壓。除此之外，該轉換器能夠依據湧浪電壓大小對疏濬能力做出調節，進而避免過大的疏浚能力造成不必要的電源重置程序或甚至是系統因過低的電源電壓而暫時性失效。

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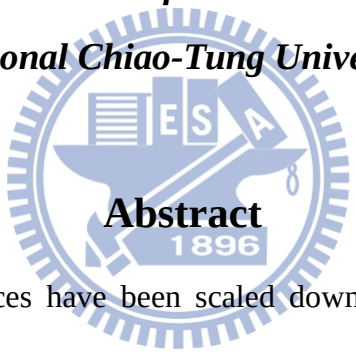

Abstract

Since the CMOS devices have been scaled down and integrated into ICs for high-speed and low-power applications, the reliability issues due to system-level ESD and surge, such as electromagnetic interference (EMI) and electrical overstress (EOS) of the CMOS ICs have become more and more important. To component-level, the devices are more vulnerable to overstress voltage or current; to system-level, the reduced voltage levels of logic gates, such as 3.3 V become 1.8 V or even lower, the noise margin (defined as $V_{DD}/2$) of logic gate against the EMI is also degraded. Therefore, the protection of system-level ESD events and surge events become significant.

There are two corresponding international standards for identifying these reliability issues in end user environment which are IEC 61000-4-2 of system-level ESD immunity test and IEC 61000-4-5 of surge immunity test. The fast transient

disturbances induced by system-level ESD and the overstressed voltage and current caused by surge events can be randomly coupled into power lines and I/O pins and malfunction the microelectronic products or even damage the devices in CMOS ICs. In order to improve the system stability, this thesis has proposed an on-chip transient detection circuit for system-level ESD protection and an on-chip surge-to-digital converter for surge protection.

It has been proven that the on-chip transient detection circuit co-design with firmware can effectively improve the immunity of CMOS ICs against the system-level ESD events. In this thesis, an on-chip transient detection circuit without using any resistor and capacitor is proposed and fabricated in a 0.18-μm CMOS process. The proposed transient detection circuit has been verified by HSPICE simulations and measurements that can successfully detect the system-level ESD disturbances. Through the cooperation with firmware programming, the system processor can judge if the system is risked by system-level ESD by the result of the transient detection circuit and perform the recovery procedure. Therefore, the microelectronic product can achieve the specification of “Class B.” when the system-level ESD events occur.

In addition to the transient detection circuit for system-level ESD, an on-chip surge-to-digital converter has been proposed in this thesis. The surge-to-digital converter has been fabricated in a 0.18-μm CMOS process. Through the HSPICE simulations and laboratory measurements, the proposed converter can successfully detect the occurrences of the surge events. It can also be applied in an on-chip surge protection against the surge-induced overstressed pulses. Besides, the converter with the configuration of output digital code dependent on surge levels can prevent the microelectronic system from unwanted power-on reset process or system dysfunction caused by excessive dissipating capability.