國 立 交 通 大 學

電子研究所

碩 士 論 文

應用於抑制癲癇發作之

雙模式刺激器系統設計

Design of Dual-Mode Stimulus System

for Epileptic Seizure Suppression

研 究 生：顏鼎洋　　(Ting-Yang Yen)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一○五年十月

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摘要

癲癇是一種神經系統疾病，通常是腦病變造成的腦細胞突然異常的過度放電。這種狀況進而引發其他部位的異常放電，而產生癲癇發作。而世界上約有 1%的人口(六千五百萬人)患有癲癇，近 80%的病例都發生在發展中國家，且發病率隨年齡增長而增高。

隨著科技演進，功能性電刺激技術已廣泛用於醫療用途。功能性電刺激（Functional Electrical Stimulation）指利用一定強度的電流，藉由刺激脈波來刺激神經或者肌肉，誘發肌肉運動或模擬正常的自主運動。功能性電刺激協助患者的肢體動作功能可以重建，而使患者回復正常肢體功能。

目前大部分功能性電刺激的方式都是利用定電流刺激，而在本篇論文則提出雙模式刺激的方式，也就是使用定電壓與定電流刺激。此刺激器晶片在電流模式能輸出 0.1mA~5mA，在電壓模式則可以輸出 0.5V~10V 的刺激大小。此外，因為電極以及人體組織阻抗會隨著電極擺放位置以及電極的大小而有所不同，加上考慮刺激規格所需的電流與電壓，因此刺激器系統還整合了電荷幫浦電路，能將 5V 輸入電壓升壓至 18V 輸出電壓供給刺激器系統做使用。

目前市面上的功能性電刺激器儀器都具有雙模式刺激的功能，將這些儀器晶片化將帶有體積與成本方面的優勢。並且，對於不同的病理需求如:癱瘓抑制、人工電子耳、帕金森氏症，運用不同的刺激方式可以達成不同治療效果，可藉此探討每種症狀較佳的刺激模式與方式。

Design of Dual-Mode Stimulus System for Epileptic Seizure Suppression

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Institute of Electronics
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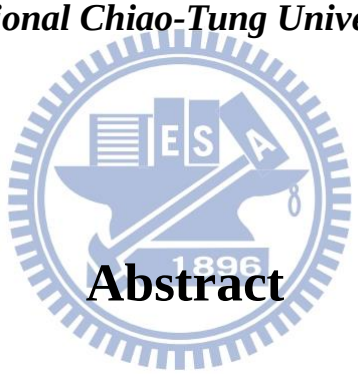

Abstract

Epilepsy is a neurological disease, usually caused by cells of brain abnormally excessive discharge. This situation will lead abnormal discharge of other parts, and induce seizures. About 1% of the population (six thousand and five hundred million) in the world suffer from epilepsy, nearly 80% of cases occur in developing countries, and the incidence increased with age.

With the evolution of technology, functional electrical stimulation technology has been widely used for medical purposes. Functional electrical stimulation refers to using of certain current amplitude and use pulse to stimulate nerves or muscles, it can induce muscle movement or simulate normal voluntary movement. Functional

electrical stimulation helps the motor function of patients can be rebuilt and the patients can return to normal limb function.

At present, most of functional electrical stimulation are using constant current stimulation method, and in this thesis has proposed the dual mode stimulation method, that is, using of constant voltage and constant current stimulation. This stimulator chip can output 0.1mA ~ 5mA in current mode, and generate 0.5V ~ 10V in voltage mode. In addition, the impedance of electrode and tissue as the electrode size and placement of the electrodes varies, with consideration of the current or voltage required to meet the stimulation specifications, thus stimulator system also integrate the charge pump circuit which is capable of boosting the input voltage 5V to 18V output voltage to supply the whole stimulator system.

Most functional electrical stimulation instrument currently on the market have a dual-mode function, and to wafer these instruments will advantage of volume and cost. Besides, for different pathological needs such as: epilepsy suppression, cochlear implants, Parkinson's disease, using of different stimulation method can achieve different treatment effects, and investigate each symptom preferred stimulus patterns and methods.

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首先要感謝在碩士班這兩年，我的指導教授-柯明道教授，感謝老師不管在學業、研究、生活、做人處事方面都給了我們許許多多寶貴的經驗以及意見，尤其在學術研究方面，老師總是能提供有效且精闢的建議。也感謝生醫各項計畫中給予我許多幫助的貴人，像是吳校長實驗室的錢信宏學長、鄭丞翔學長。

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顏　鼎　洋

誌於竹塹交大

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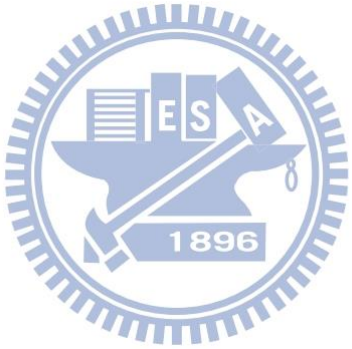


Chapter 1
Introduction

1.1 Motivation

The patients who were suffering from nervous diseases only can treat by few methods in the past. Fortunately, biomedical and electronics technology grow up rapidly, there are more and more treatment methods can be used to cure nervous diseases. Biomedical technology already developed several applications such as X-ray, magnetic resonance imaging (MRI) [1], electroencephalography (EEG) [2], electrocorticography (ECoG) [3], physiological sensor [4], even biomedical implant SOC [5] are applied and these are helpful to patients and doctors in the surgery. According to the research of the neuroscience, some lose physical functions can restore by functional electrical stimulation (FES) [6]. For instance, retinal prostheses for treating blindness [7], cochlear implants for treating hearing damage [8], spinal cord stimulation for restoration of motor functions [9], deep brain stimulation for treating parkinson's disease [10]. Furthermore, epilepsy is also one of diseases investigated to be treated by functional electrical stimulation.

Epilepsy is a chronic neurological disease, and it characterized by epileptic seizures. Epilepsy can have both genetic and acquired causes, with interaction of these factors in many cases. However, in sixty percent of cases, epilepsy are all unknown etiology. There are still some more recognized causes: excessive drinking, head trauma, light stimulation, lack of sleep and emotional. It will cause patients inattentive, feeling dazzle, winking eyes or self-mumbling. Approximately 1% of the world’s population (60 million people) suffer from epilepsy. Therapies of epileptic seizure

include pharmacologic treatment and surgical treatment. The first step will be the pharmacologic treatment. For patients who do not respond to the medicament pharmacologic treatment, the surgical treatment will be used. However, the surgical treatment is irreversible treatment and might cause important physiological functions loss, hence the surgical treatment should use more precise method to analyze current situation. When the patients need surgery, the doctor will use EEG technology to analyze the probable disordered position which is seizure-onset zone can be found and the source of abnormal discharge tissue position can be predicted before seizure [11]. Next, the doctor will perform ECOG. Because ECOG is using method of intracranial electrodes detection, it can confirm a more accurate seizure-onset zone. Brain mapping [12] will be performed after ECOG. During brain mapping, doctors will stimulate each electrode on the cerebral cortex. According to the response of patient, doctors can find seizure-onset zone location, maybe on the cortex such as primary motor cortex or primary sensory cortex. If the seizure-onset zone is not on the important region, doctors will do resection surgery. But the seizure-onset zone of every patient is not always at safe region, so alternative plan is needed. It also has been mentioned that the abnormal discharge signal that causes epilepsy can be suppressed by FES when detecting the abnormal brain wave [13]. Moreover, finding out the location of abnormal source tissue can have more high probability to suppress seizures. So our ultimate goal is design the stimulator system for biomedical application.

Compared FES to the surgical treatment, the advantages of electrical stimulation treatment are more flexible, recoverable and do not damage the brain tissue, but there are still several challenges in designing the electrical stimulation system. First, the equivalent circuit of electrode and tissue will vary in a wide range because of different sizes, locations, and material of electrodes. The stimulus current to suppress epileptic

seizures in this design is up to 5mA. In addition, the series resistance of equivalent impedance (Rs) is about 1kΩ~3kΩ. If considering the worst case that is equivalent impedance is 3kΩ and stimulus current is 5mA, so the stimulator system need high voltage generator to produce more than 15V for supplying stimulus driver. Moreover, not only epileptic seizures suppression application but also for more stimulation applications in biomedical field, so the design of stimulator system also can realize two modes of stimulation: current mode and voltage mode. In current mode stimulator system is able to generate 0.1mA to 5mA (per 0.1mA step), and in voltage mode is able to generate 0.5V to 10V (per 0.5V step). Because the highest voltage in this chip is about 18V, this work needs to be implemented in high-voltage process. Implementing chip in high-voltage process can overcome the N-well/P-sub interface breakdown problem. The problems of gate-oxide overstress, hot-carrier effect, and other reliability issues will be considered [14]. In this thesis, the proposed dual mode stimulus driver and high voltage generator are realized.

1.2 Thesis Organization

The first chapter illustrates the motivation of this work and the thesis organization.

Chapter 2 shows background of epilepsy, epileptic seizures treatment and implantable closed-loop neural prosthetic SoC for suppressing epileptic seizure.

Chapter 3 explains design of dual mode stimulus driver for epileptic seizure suppressing in detail, and the proposed dual mode stimulus driver had been implemented in the 0.25μm HV USG 2.5V/5V/12V process.

In chapter 4, as mentioned above the stimulator system needs high supply voltage, so this chapter shows the design of high voltage generator. The high voltage generator is a PFM system. In other words, if the loading current is heavier, the PFM system working frequency is higher. This high voltage generator also had been fabricated in the 0.25μm HV USG 2.5V/5V/12V process.

The last chapter, chapter 5, reviews and summarizes above chapters of this thesis, and bring some improvements in future work.

Chapter 2
Background of Epilepsy and Epileptic SoC Introduction

2.1 Overview of Epilepsy and Epileptic Treatment

Epilepsy is a chronic neurological disease of the cerebrum. According to its definition, epilepsy seizure is spontaneous and does not have direct incentives such as acute illness. Since epilepsy is a cerebrum disease, to understand cerebrum structure and the specific function of blocks can be helpful. Fig. 2.1.1 shows a brief block of cerebrum. Generally the cerebrum can be divided into four areas: frontal lobe, parietal lobe, occipital lobe and temporal lobe. Obviously they play different roles in cerebrum.

Frontal lobe is related to structure of human language, expression of human language, self-awareness and voluntary muscle control.

Parietal lobe process various types of sensory information such as pain and touch, parietal lobe is also related to language and memory function.

Occipital lobe can process visual information, such as the primary visual cortex V1 is located on occipital lobe region.

Temporal lobe is the primary and secondary auditory cortex is located, for the treatment of central auditory message.

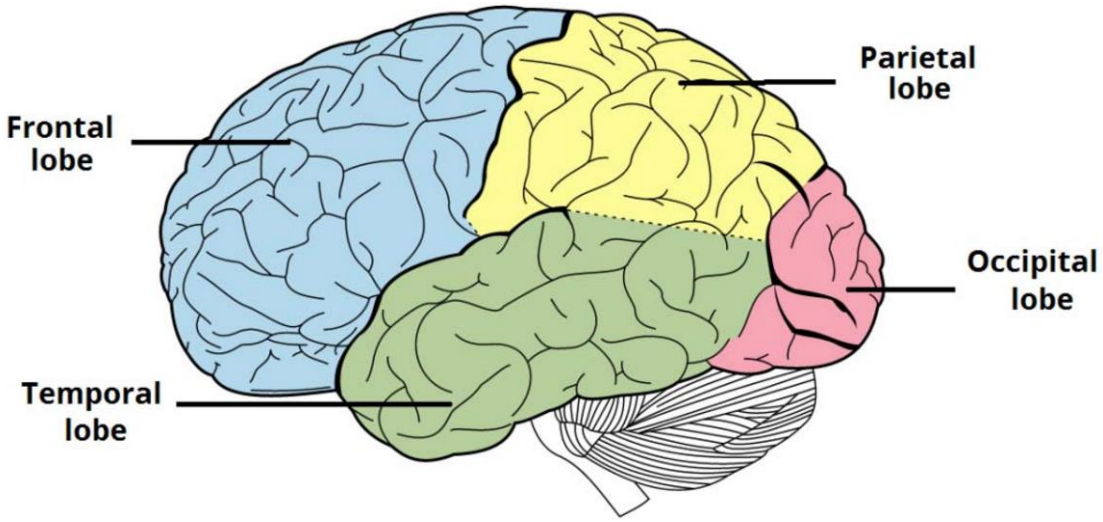


Fig. 2.1.1 Brief block of cerebrum.

The cerebrum regions are further subdivided, according to a Brodmann area which is shown in Fig. 2.1.2. A Brodmann area is a region of the cerebral cortex, in the human or other primate brain, defined by its cytoarchitecture, or histological structure and organization of cells. Many of the areas Brodmann defined based solely on their neuronal organization have since been correlated closely to diverse cortical functions. For example, Brodmann areas 1, 2 and 3 are the primary somatosensory cortex; area 4 is the primary motor cortex. Area 17 is the primary visual cortex; and areas 41 and 42 correspond closely toprimary auditory cortex.

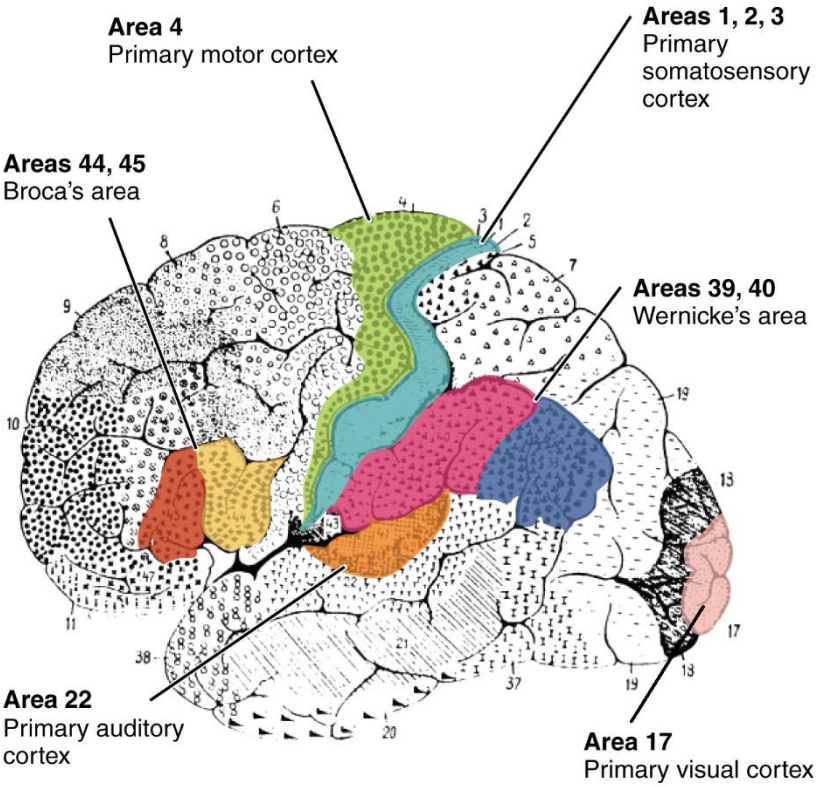


Fig. 2.1.2 Brodmann area.

For practical example and explained epileptic seizures process, Fig. 2.1.3. shows the ECOG signal of epileptic patient. The left number of figure shows the location of electrodes implanted in the cerebrum. When the patient epileptic seizures, his right hand will be proudly arched, then his whole body cramps and shakes. ECoG signal can be observed from the figure. When the seizures started, there is a number 25, 26 electrode abnormally discharge signal, as it contained a slow wave (low frequency) signal. Then this abnormal signal will induce other position become abnormal state, then his whole body cramps and shakes. According to a Brodmann area, the abnormal discharge position is located in the junction of motor cortex and the sensory cortex. If stimulate number 25, 26 electrode of patient, it will react to the hand of patient. This also verifies location of number 25, 26 electrode correspond to the definition of Brodmann area.

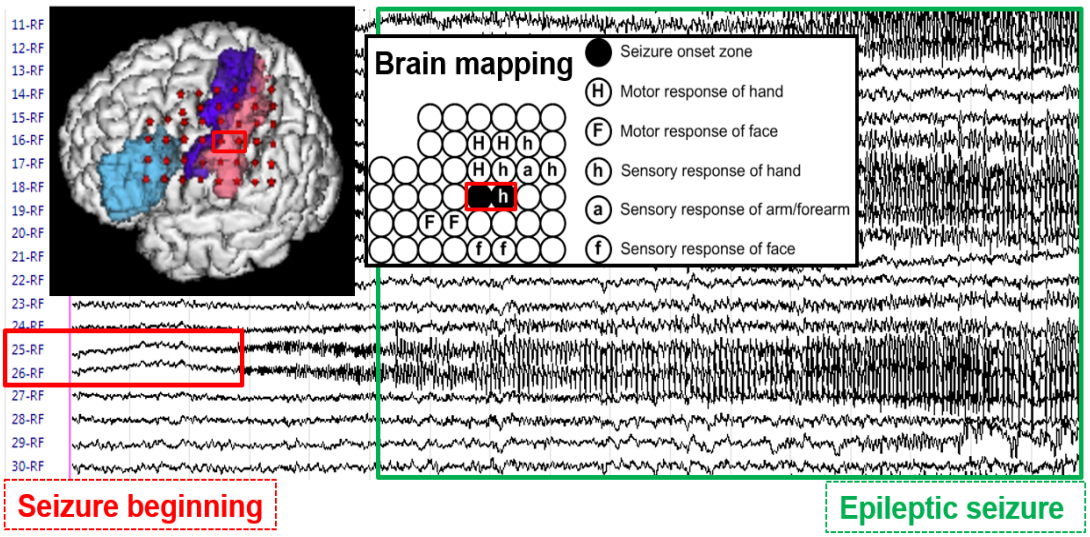


Fig. 2.1.3 The ECoG signals of a clinical example.

As mentioned above, the first step will be pharmacologic treatment. About 20% to 30% of epileptic patient are ineffective to pharmacologic treatment. For patients who do not respond to the medicament pharmacologic treatment, the surgical treatment will be used. But the surgical treatment is more dangerous and risky. When the patients need surgery, analyzing the probable disordered position which is seizure-onset zone by using EEG technology is very important. Then using ECOG to confirm a more accurate seizure-onset zone. Brain mapping will be performed after ECOG. If the seizure-onset zone is not on the important region, doctors will do resection surgery. Unfortunately, the seizure-onset zone of every patient is not always at safe region, so perform FES to suppress epilepsy also is alternative choice. Moreover, finding out the location of abnormal source tissue can have more high probability to suppress seizures. The whole process of epileptic treatment is show in Fig. 2.1.4.

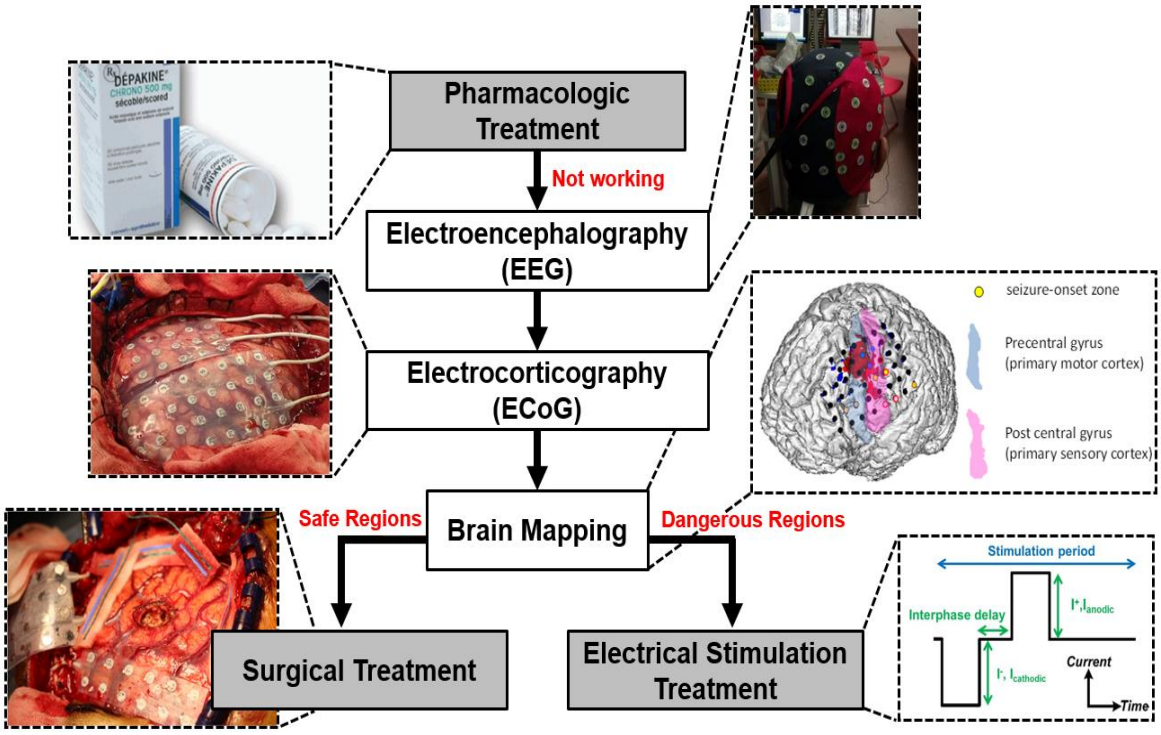


Fig. 2.1.4 The steps of epileptic treatment.

2.2 Closed-Loop SoC for Suppressing Epileptic Seizure, and The Considerations and Methods of Stimulation

2.2.1 Closed-Loop SoC for Suppressing Epileptic Seizure

Fig. 2.2.1 shows the block diagram of the closed-loop SoC for suppressing epileptic seizures [15]. The system consists of external chip and implanted chip. The SoC has several function system such as power system, communication system and stimulator system.

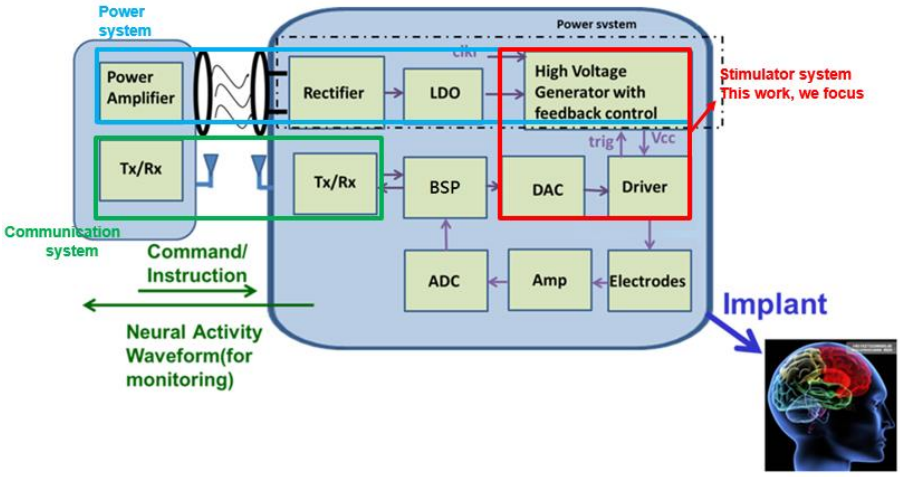


Fig. 2.2.1 The block diagram of an implantable SoC example.

This SoC enlarges physiological signals through electrodes and pre-amplifier, then the enlarged signals are sent to input of ADC. The analog physiological signals are converted into digital signals, and these digital signals will be processed in time-domain or frequency-domain by Biomedical Signal Processor (BSP). Then BSP will control stimulator to do current stimulation for suppressing epileptic seizures. The information of which channels are select, the value of stimulation current and control of ANO, CATH and Discharge signals are also generated by BSP.

Moreover, the recorded ECoG signals can be transmitted by Tx/Rx to monitor system. The ECoG data can be provided to doctor for using in future. Because of Tx/Rx transmission system, taking out the internal SoC to adjust stimulation parameter is non-essential. In addition,data transmission is encoded through a reliable cyclic redundancy check (CRC). If the data transmission is not pass the CRC, the system will pass the data to ensure the accuracy of data.

The power system consists of power amplifier, rectifier, LDO, and high voltage generator (charge pump). In the external part, the power amplifier transmits the power through the way of LC resonance. In the implanted part, the rectifier converts the AC

to DC from secondary coil and low dropout regulator (LDO) converts the output voltage of rectifier to a more stable voltage source which supplies to the input of charge pump of implanted part. Then the high voltage generator will pump to about 3~4 times of input voltage (from LDO) for stimulator using.

The wireless system can be transmitted of the industrial scientific medical band (ISM) which is 13.56MHz.

2.2.2 Introduction of Functional Electrical Stimulation (FES)

Functional electrical stimulation refers to using of certain current amplitude and use pulse to stimulate nerves or muscles, it can induce muscle movement or simulate normal voluntary movement. Functional electrical stimulation helps the motor function of patients can be rebuilt and the patients can return to normal limb function [16].

FES systems conventional biphasic stimulus waveforms shown in Fig. 2.2.2. This is more common stimulation method: current mode stimulation. The waveform of electrical stimulation pulse is characterized by three parameters: amplitude, pulse width, and pulse frequency. For different clinical applicatons, each of the parameters may be different. First, the cathodic current usually starts to elicit a desired neural response, while the anodic current. Second, the interphase delay separates the currents so that the anodic current does not reverse the physiological effect of the cathodic current. Final, the cathodic current cancels due to anodic/cathodic current mismatch on electrode pair.

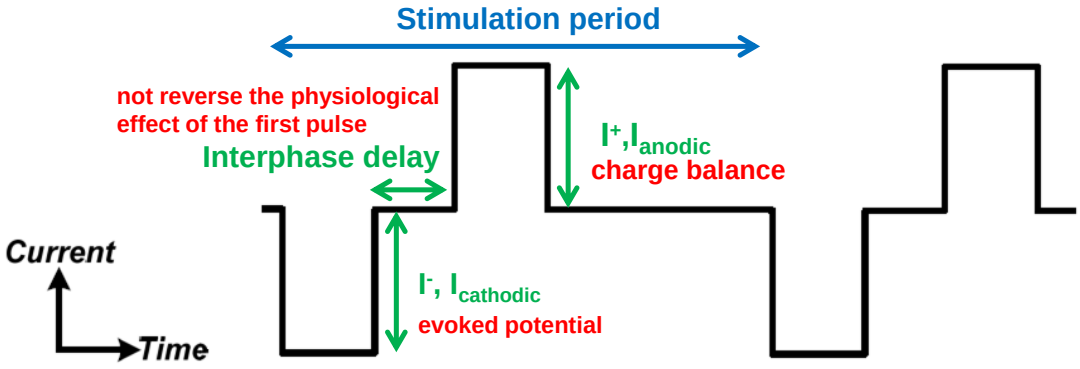
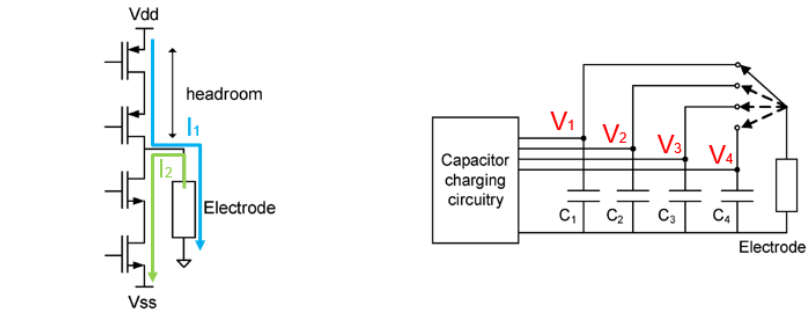


Fig. 2.2.2 Conventional biphasic stimulus pattern in current mode.

2.2.3 Considerations and Methods of Stimulation

As mention above, stimulation can generally be divides into two methods: current mode and voltage mode.

Fig. 2.2.3. shows the brief demonstration of two methods. The left part of figure is current mode, the one side of electrode always connect to ground. Using positive, negative and control of switch to generate cathodic current (I_2) and anodic current (I_1). Relatively, the left part of figure is voltage mode, it used different sample capacitances and control of switch to different voltage on the electrode.



(a) Current-mode stimulation (b) Voltage-mode stimulation

Fig. 2.2.3 The brief demonstration of two methods.

Fig. 2.2.4. shows the example of current mode stimulation [17]. This example used the current mirror (Mp2 and MP1) to generate output current, and the switch (Mp3 and Mn2) to decide stimulate or not. Moreover, the stimulator system also have adaptor to sense output current. If the output current is higher, the Vcontrol will go higher, making charge pump to pump to higher voltage. This mechanism can improve overall efficiency of stimulator system.

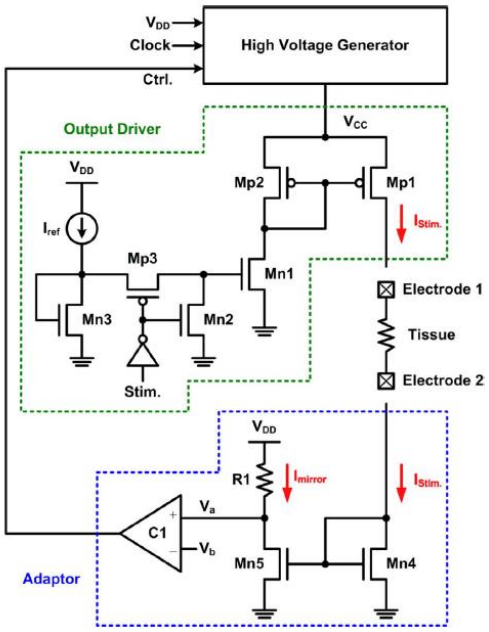


Fig. 2.2.4 The example of current mode stimulation.

Fig. 2.2.5. shows the example of voltage mode stimulation [18]. The example sampled different voltage on different capacitances, and used switch to apply positive or negative voltage on electrodes.

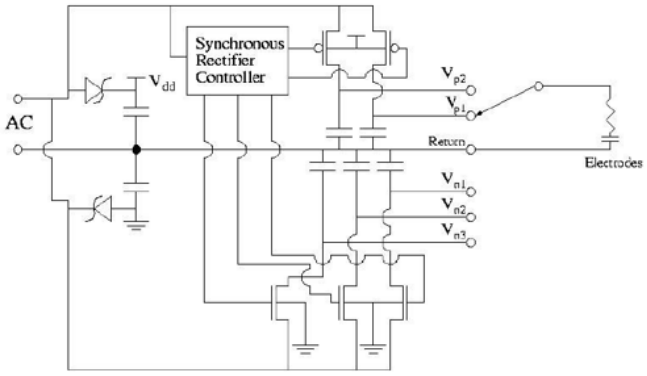
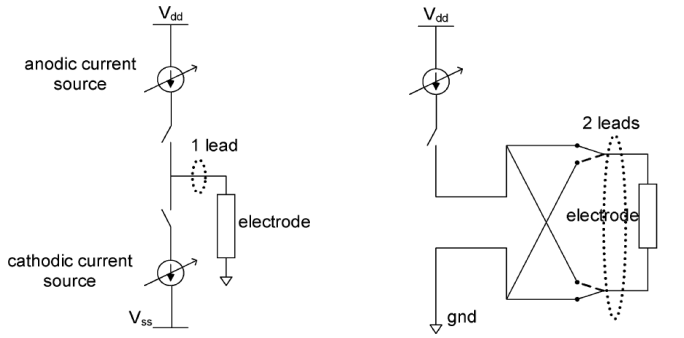


Fig. 2.2.5 The example of voltage mode stimulation.

To generate the biphasic current pulses, there two configurations of chip-electrode interface for each stimulation site: one interface lead per site (monopolar stimulation) and two interface leads per site (bipolar stimulation) [19].

Fig. 2.2.6(a) shows the configuration of one interface lead per site (monopolar stimulation), when the monopolar stimulation is used, two supply voltages are required to provide the cathodic and anodic stimulus currents. And a return electrode side is connected to the ground potential in this case.

Similarly, Fig. 2.2.6(b) shows the configuration of two interface lead per site (bipolar stimulation), when the bipolar stimulation is used, only one supply voltage is required. The anodic and cathodic stimulus currents are provided by reversing the current paths by switching the MOSFETs.



(a) One Interface lead per site (Monopolar Stimulation)

(b) Two Interface leads per site (Bipolar Stimulation)

Fig. 2.2.6 Different stimulation method in current mode.

Fig. 2.2.7 is an example of monopolar stimulation [20]. As mentioned above, the positive high voltage (+5V) and negative high voltage (-5V) are required to generate cathodic and anodic stimulus currents. To solve the current mismatch problem, this work use self-calibration technique to minimize the unbalance of charge due to current mismatch between the anodic and the cathodic pulses. The result is that maximum stimulus current is 1mA, and less than 0.3μA current mismatch. And the chip is realized in the 0.35μm high voltage CMOS process.

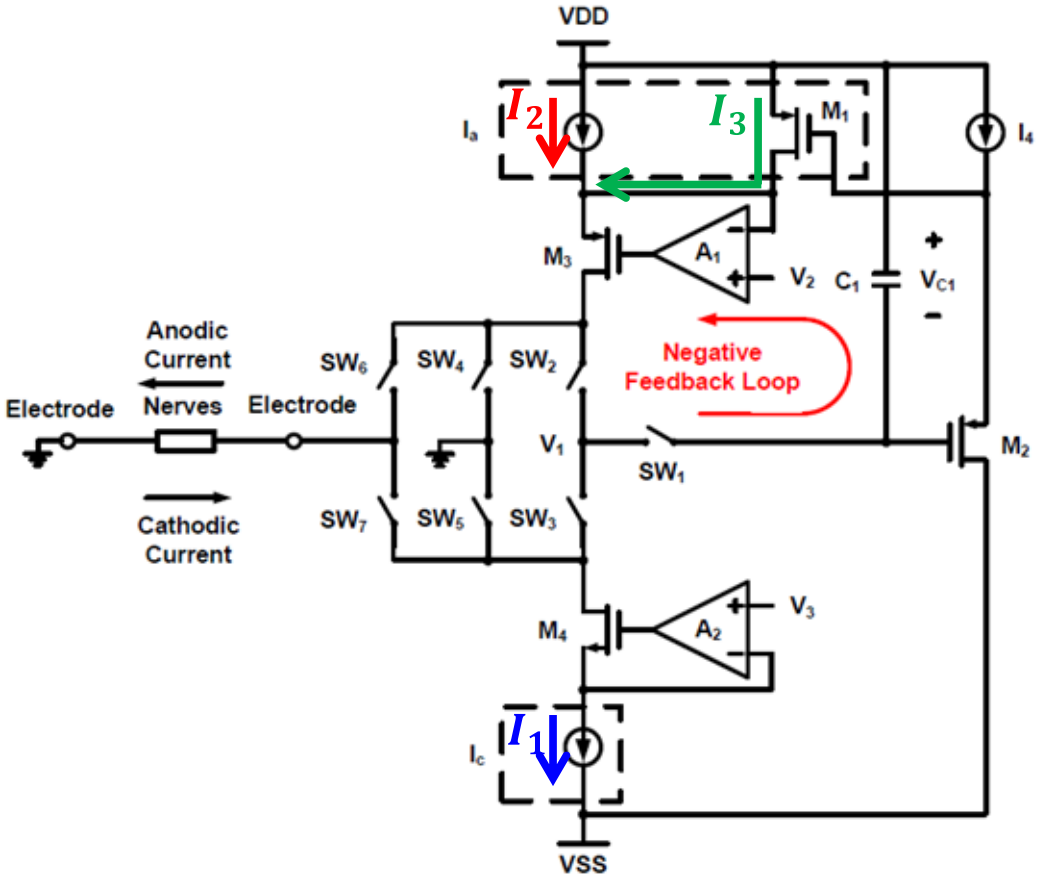
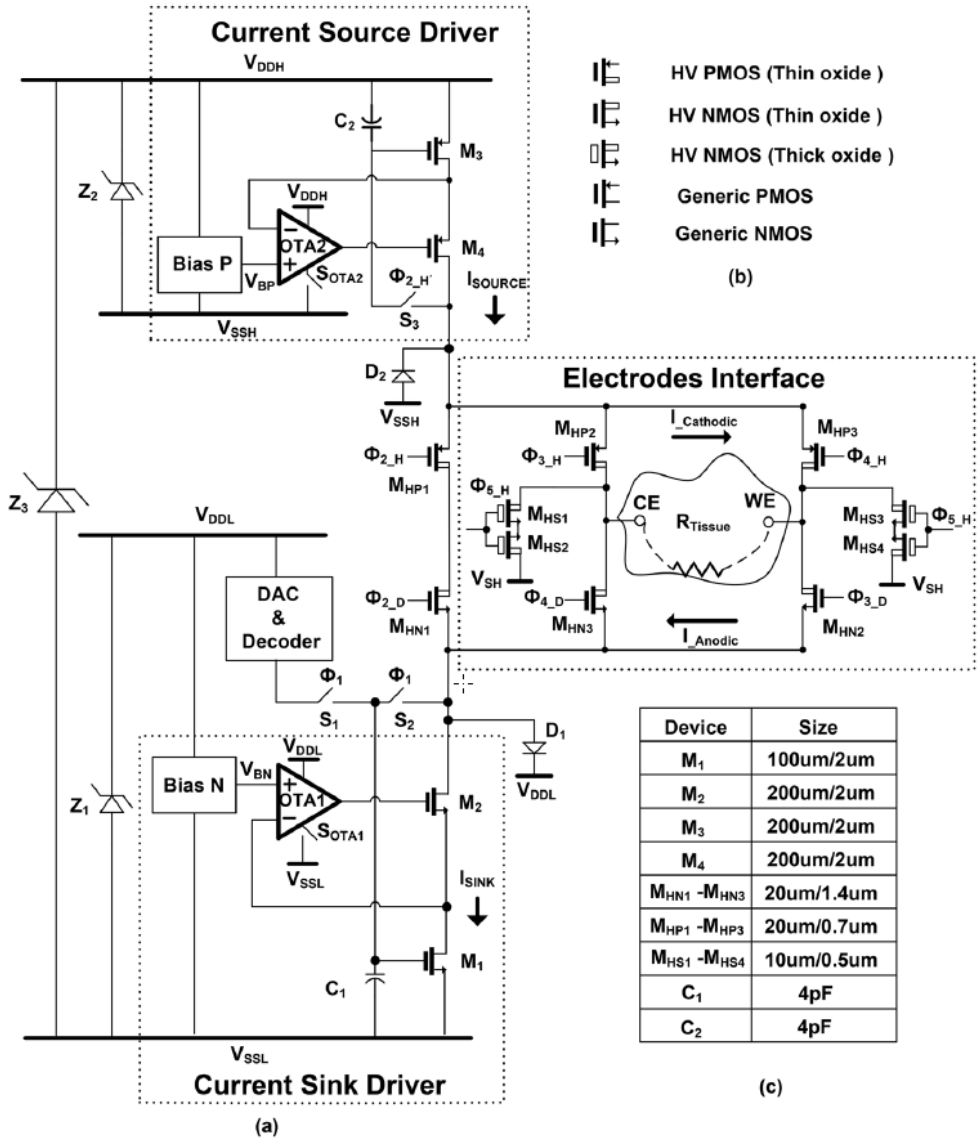


Fig. 2.2.7 One interface lead per site example in current mode.

Fig. 2.2.8 is an example of bipolar stimulation [21]. The system operates at 15V high supply voltage and controls transistors M_{HP2}, M_{HP3}, M_{HN2}, and M_{HN3} as switches for anodic or cathodic current paths. Similarly, to solve the current mismatch problem, using dynamic current mirror to sample current source and current sink through capacitance C_1 and C_2. The result is that maximum stimulus current is 1mA, and less than 3μA current mismatch. And the chip is realized in the 0.35μm high voltage CMOS process.



Device	Size
M_1	100um/2um
M_2	200um/2um
M_3	200um/2um
M_4	200um/2um
M_{HN1} -M_{HN3}	20um/1.4um
M_{HP1} -M_{HP3}	20um/0.7um
M_{HS1} -M_{HS4}	10um/0.5um
C_1	4pF
C_2	4pF

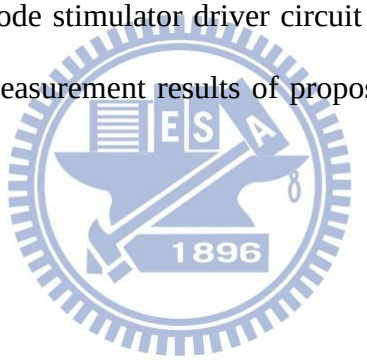
Fig. 2.2.8 Two interface leads per site example in current mode.

Chapter 3

Design of Dual-Mode Stimulus Driver for Epileptic Seizure Suppression

3.1 Introduction

In this chapter, the illustration is separated into three parts. First, our purpose is realizes stimulator system for epileptic seizure suppression. Therefore, impedance of brain tissue analysis is absolutely needed. We will use instrument to do this work. Second, the ideal of dual mode stimulator driver circuit is demonstrated in this part. Third, the simulation and measurement results of proposed stimulator driver will be presented in this part.



3.2 Design Background of Stimulus Driver

3.2.1 Impedance Analysis

The electrode-tissue impedance can be modeled by Fig. 3.2.1. according to [22][23]. In this simplified model, R_S is the solution spreading resistance, which is determined by the resistivity of the two electrodes (including the resistivity of solution). C_{dl} is the double-layer capacitance, which represents the ability of the electrode to cause charge flow in the electrolyte without electron transfer. R_f is the Faradaic resistance, which is represents the Faradaic processes of reduction and oxidation where electron transfer occurs between the electrode and electrolyte. If the net charge on the metal electrode is forced to vary (as occurs during stimulation), a

redistribution of charge occurs in the solution. Suppose that two metal electrodes are immersed in an electrolytic salt solution. Next, a voltage source is applied across the two electrodes so that one electrode is driven to a relatively negative potential and the other to a relatively positive potential. At the interface that is driven negative, the metal electrode has an excess of negative charge (Fig. 3.2.2).

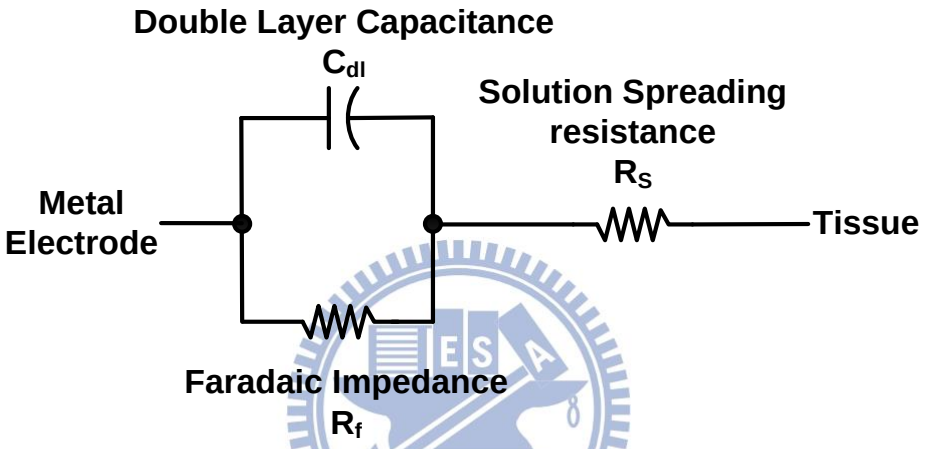


Fig. 3.2.1 The equivalent impedance of electrode-tissue.

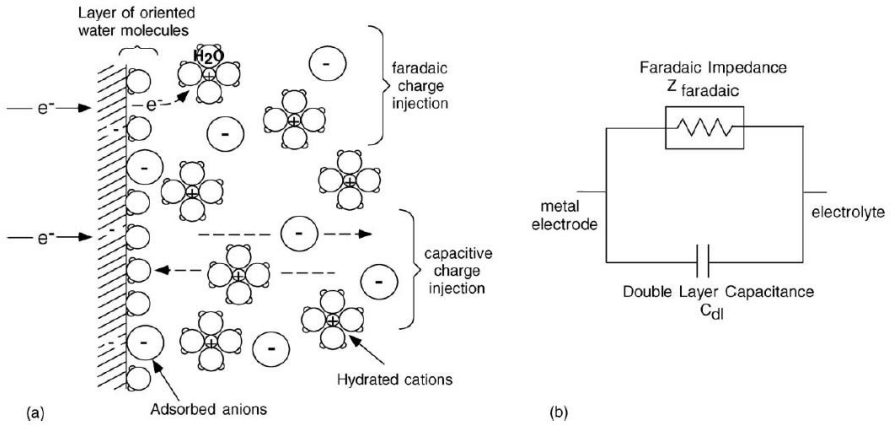


Fig. 3.2.2 The electrode/electrolyte interface: (a) physical representation; (b) two-element electrical circuit model for mechanisms of charge transfer at the interface.

In this section, we measured the equivalent impedance of real brain tissue. The measurement setup is shown in Fig. 3.2.3. We used Solartron SI 1260A Impedance Analyzer to analyze impedance of real brain tissue. Just like setup is shown in Fig. 3.2.3, the brain tissue attached to medical electrode, and the medical electrode connected to SI 1260A through the connector. The enlarged photo of brain tissue is shown in Fig. 3.2.4. The electrode used in this case is AD-TECH IS04R-SP10X-000. The area of cerebral cortex is probable 1×1.5 cm^2 and the electrode is used by which is platinum material (charge density limit 100~150μC/cm^2) and has 2.3mm diameters of contact area to measure the equivalent impedance (Picture is shown in Fig. 3.2.5). The impedance analyzer sweeps frequency from 1 to 10^6 Hz and the sets ac amplitude 1V (Fig. 3.2.6).

We will get the measurement result curve, and using the software to fit the curve, then obtain the equivalent impedance finally. The result of the impedance measurement is shown Fig. 3.2.7. The RS is 2.874kΩ, Cdl is 742nF, and Rf is 341kΩ.

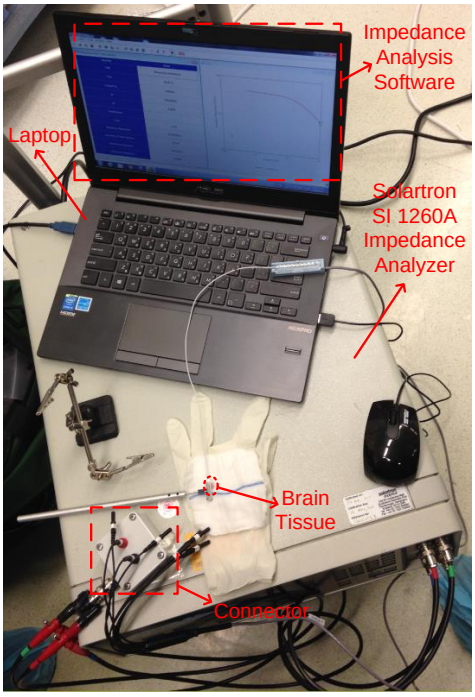


Fig. 3.2.3 The measurement setup of impedance analysis.

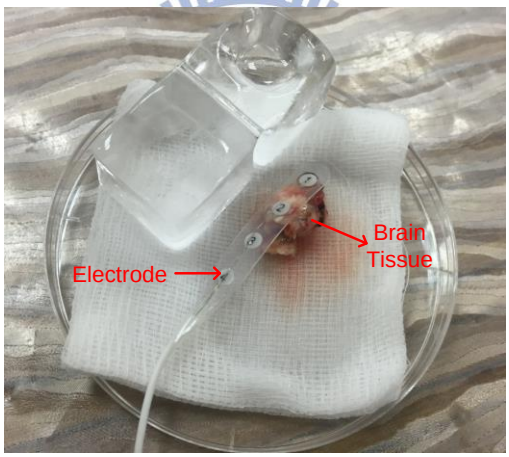


Fig. 3.2.4 Zoom in photo of brain tissue.

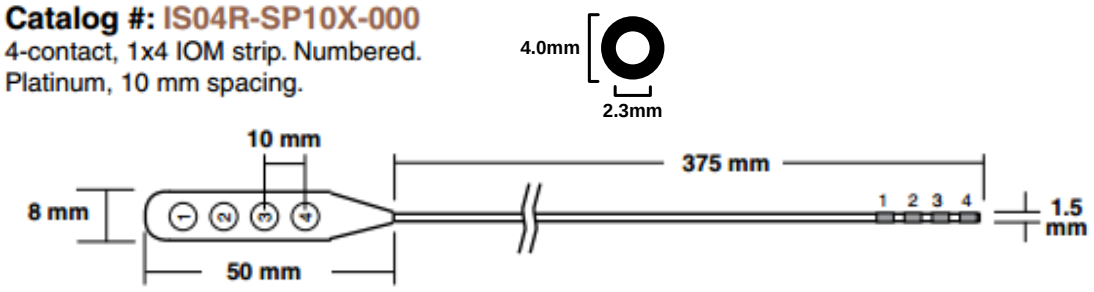


Fig. 3.2.5 AD-TECH IS04R-SP10X-000 electrode.

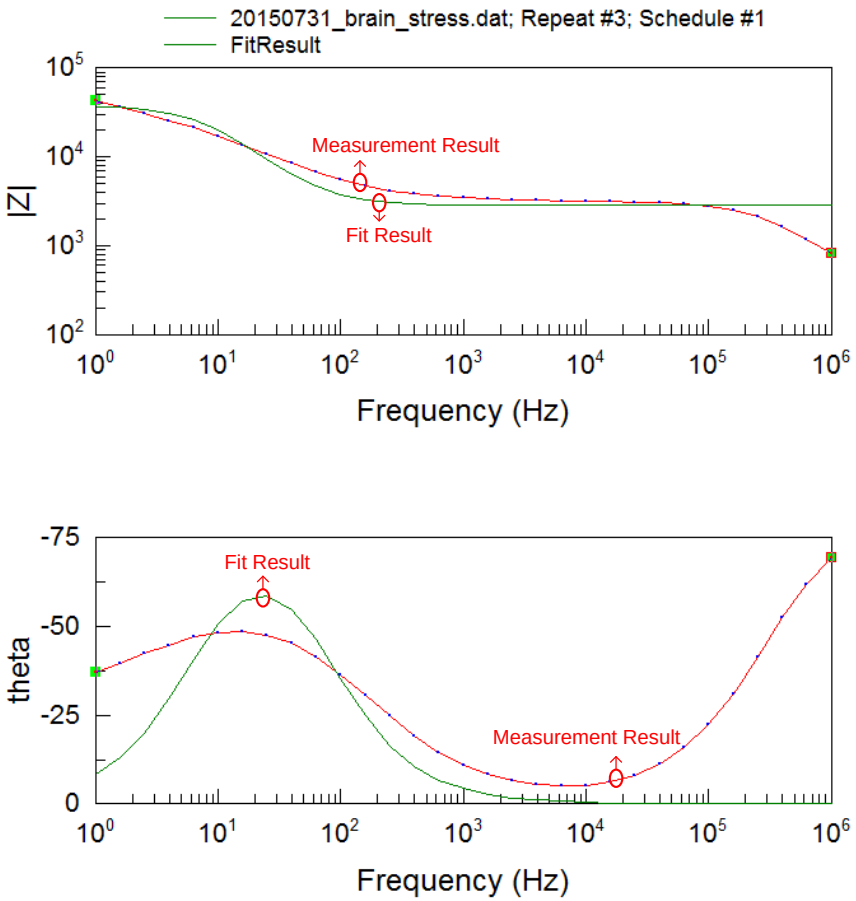
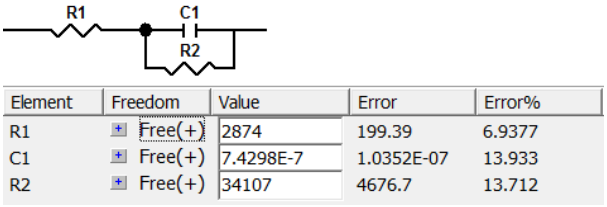


Fig. 3.2.6 The fitting result of impedance measurement.



Element	Freedom	Value	Error	Error%
R1	Free(+)	2874	199.39	6.9377
C1	Free(+)	7.4298E-7	1.0352E-07	13.933
R2	Free(+)	34107	4676.7	13.712

Fig. 3.2.7 The equivalent impedance model.

3.2.2 Specifications of Dual-Mode Stimulus Driver

First of all, we have to decide the specifications of dual mode stimulus driver. For covering wide application range of biomedical stimulus systems and variable impedance of physiological tissue [24], the specification of maximum stimulus current is set to 5mA and 0.1mA per step. Considering the solution spreading resistance R_S is about 3kΩ, therefore in the voltage mode, maximum stimulus voltage is set to 10V. In this stimulus voltage can cause equivalent current about 3mA through the tissue and reach effective stimulation. Moreover, R_S of the equivalent impedance is about 3kΩ and the maximum stimulus current is up to 5mA which can cover wide application range of biomedical stimulation, the high voltage supply of stimulus driver needs higher than 15V. In this chip, we also design the high voltage generator which can generate 18V from 5V input. This DC-DC converter will be illustrated in detail in Chapter 4. The electrode configuration is bipolar type (two leads per site).

Moreover, traditional 0.18μm process cannot sustain 18V condition. Under 18V condition its N-well/p-sub interface will breakdown. So, this chip uses 0.25μm HV USG 2.5/5/12V process to realize. The power dissipation in an implanted stimulator is also an important issue. Large power dissipation will cause temperature rise in 1°C~ 2°C above the normal human temperature. It could lead to the physiological damage. Therefore, the standby power must be less than tens of mW. The summary of the specifications of dual mode stimulus driver is shown in the Table 3.1.

Table 3.1
Specifications of stimulus driver.

Process	0.25-μm HV USG 2.5/5/12V Process
Electrode Configuration	Bipolar (two channels per site)
Supply Voltage	2.5V & 5V
Current-Mode Stimulation Amplitude	0.1mA ~ 5mA (0.1mA per step)
Voltage-Mode Stimulation Amplitude	0.5V ~ 10V (0.5V per step)
Output Resistance Load	1kΩ ~ 3kΩ
Channel Number	4 channels
Power Consumption	Minimum

3.2.3 Introduction of 0.25μm High Voltage USG 2.5/5/12V Process

As mentioned above, because of the highest voltage operation about 18V, so we chose 0.25μm HV USG 2.5/5/12V process to realize stimulus chip. In this process, we used three different MOS device. Table 3.2 shows the 2.5V NMOS/PMOS standard device and the 5V NMOS/PMOS I/O device. The 2.5V device and the 5V device most different point is the type of the gate oxide, the gate oxide of 5V device is using OD2 layer. Compared to OD1 layer using in 2.5V device, OD2 layer is more thick than OD1 layer, so their sustain voltage between drain, source, gate and bulk is different. The sustain voltage between drain, source, gate and bulk of 5V device is about 5V~5.5V, and the sustain voltage between drain, source, gate and bulk of 2.5V device is about 2.5V~2.75V. In order to distinguish two different device in sequence of chapter, the gate line on the left of 5V device symbol is bold, and the gate line on the

left of 2.5V device symbol is fine. Moreover, the process N-well/P-sub interface breakdown voltage is 18.5V. This breakdown voltage limit is inherent in the process.

Table 3.2

0.25μm low-voltage MOSFET cross-section view and symbol.

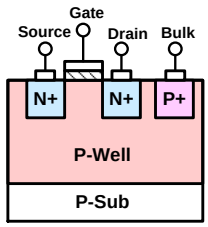
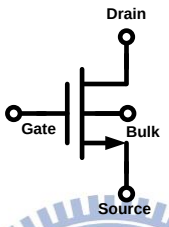
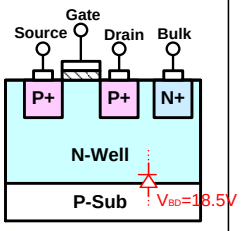
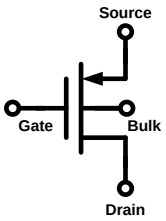
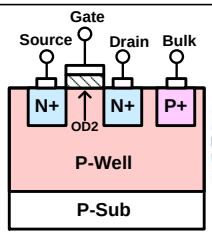
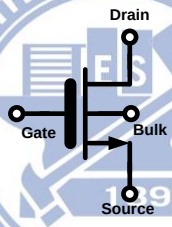
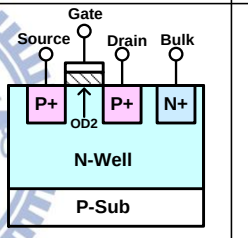
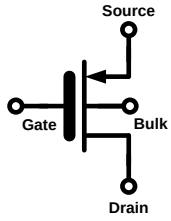
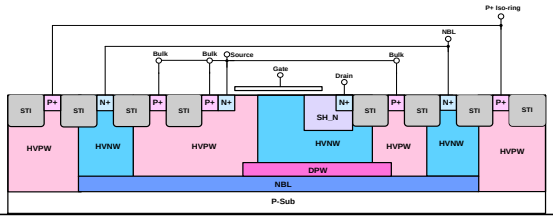
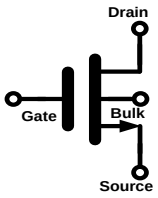
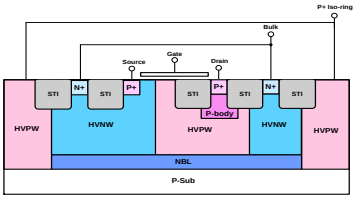
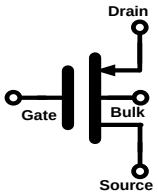
	NMOS		PMOS	
	Cross-section view	Symbol	Cross-section view	Symbol
2.5V Device				
5V Device				

Table 3.3 shows the 12V NMOS/PMOS high-voltage device. Sustain voltage between drain, source, gate and bulk of 12V device is about 12V~13.2V. Moreover, the 12V NMOS/PMOS high-voltage device are surrounded by specific layer just like HV N-Well, HV P-Well, Deep P-well and NBL. These specific layer are used to improve breakdown voltage between different interfaces. Similarly, in order to distinguish different device in sequence of chapter, the gate line of 12V device symbol are both bold.

Table 3.3

0.25μm high-voltage MOSFET cross-section view and symbol.

	Cross-section view	Symbol
NMOS		
PMOS		

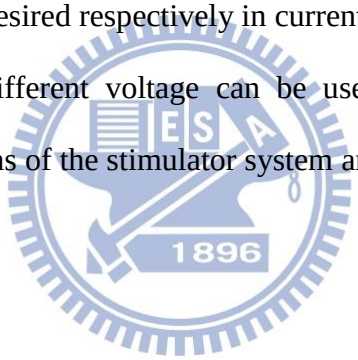
3.3 Design of Dual-Mode Stimulus Driver

3.3.1 Architecture of Stimulator System

The block diagram of the stimulator system is shown in Fig. 3.3.1. It consists of some sub-blocks, including level-shift (high-side), level-shift (low-side), stimulus drivers, bias circuit, 6-bits thermometer code DAC, current mode & voltage mode select circuit, current mirror, decoder, and high voltage generator. Also, level-shift (high-side), level-shift (low-side), stimulus driver composes stimulus unit, and there are four stimulus units (channels) in the stimulator system. The brief function of each block is explained as follow. First, the decoder will decide which two stimulus units are chosen by C [3:1] pin, operate in current mode or voltage mode by Sel_mode pin, the value of current mode or voltage mode stimulation and which channel holds priority by PRI pin. The stimulus unit play an output stage role in stimulator system. When operating in current mode, stimulus unit can force certain value of current flow from the one of chosen channel to the other one. Similarly, when operating in voltage mode, op-amp of stimulus units will drive voltage on two channels. Constant current source is using 6-bits thermometer code DAC to generate, copy and enlarge current value by current mirror block. Actually voltage mode and current mode use the same

current source, then the mode select circuit is able to decide to result current signal or voltage signal and the pin AMP [6:1] can control the current source amplitude also voltage mode amplitude. As mentioned above, the final output waveform will decide by control pins Sel_mode, ANO, CAT, PRI and Discharge. The high voltage generator can pump voltage to 4xVDDH from input voltage 1xVDDH, and this voltage is highest voltage of stimulator system. When 4xVDDH is generated, the bias circuit will respectively produce 3xVDDH, 2xVDDH and 1xVDDH. The three different voltage collocate with high-side level shift, low-side level shift, ANO signal and CATH signal (pass through decoder) are able to create required signals, the signals can control MOS switches to be turned on or turned off in proper timing, so we can get the waveform which is desired respectively in current mode or voltage mode.

Moreover, the three different voltage can be used to apply voltage limiting technique. All block functions of the stimulator system are explained above.



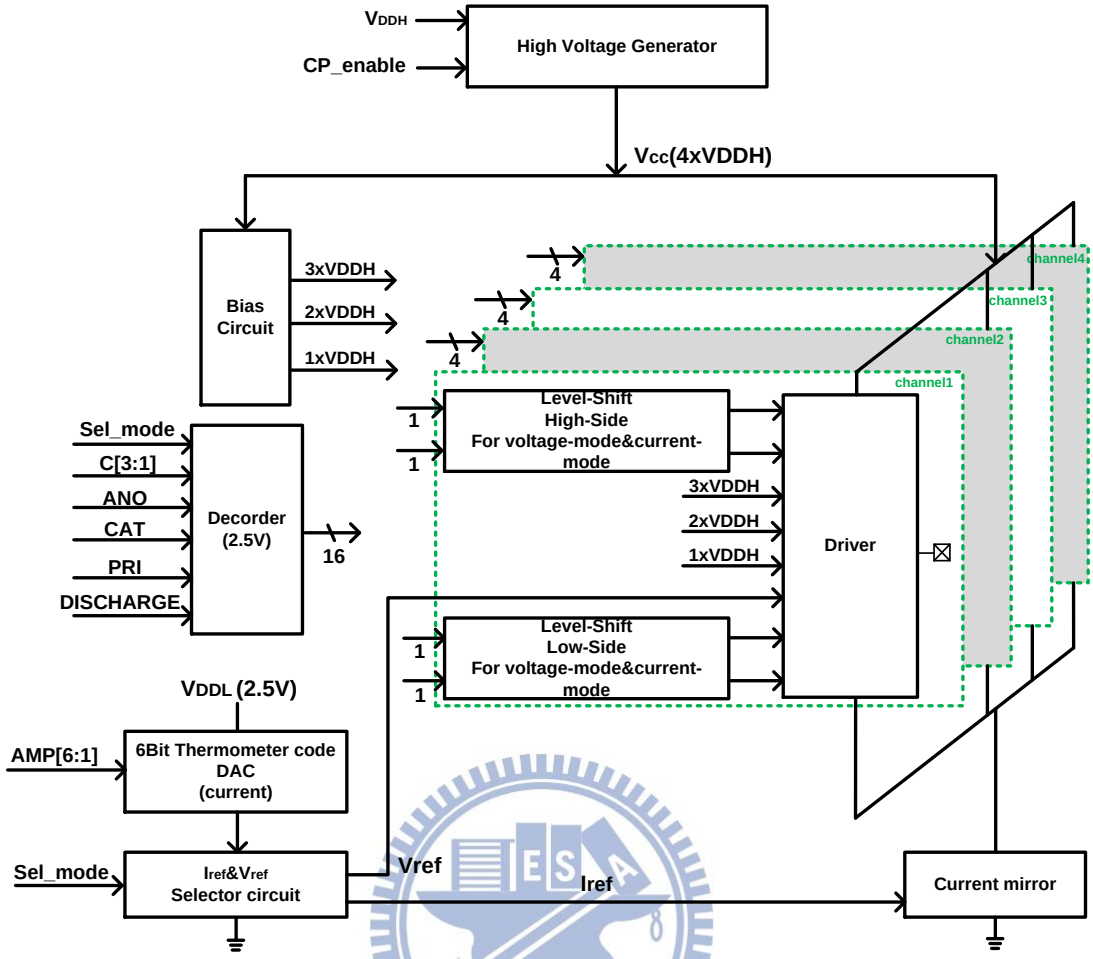
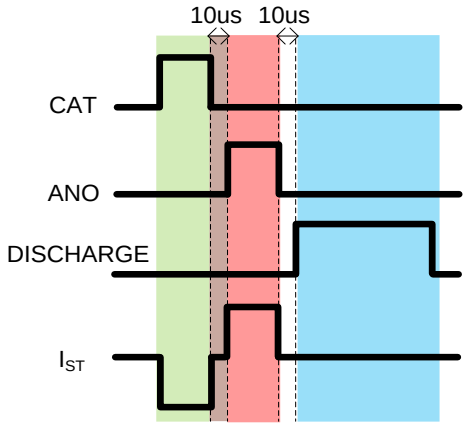


Fig. 3.3.1 The block diagram of the stimulator system.

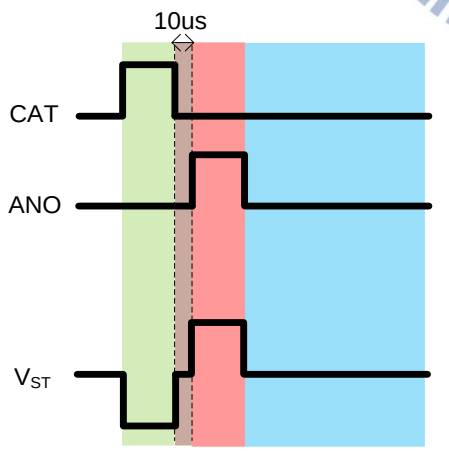
Fig. 3.3.2 shows the control signal and current level of 6-bits amplitude in current mode. The control pins ANO, CAT and DISCHARGE control the output waveform and AMP[6:1] decides the output stimulus current amplitude.



Amplitude signal AMP[6:1]	Stimulus current (Ist)
001010	1.0mA
010100	2.0mA
011110	3.0mA
101000	4.0mA
110010	5.0mA

Fig. 3.3.2 Control signal and current level of 6-bits amplitude in current mode.

Fig. 3.3.3 shows the control signal and current level of 6-bits amplitude in voltage mode. The control pins ANO and CAT control the output waveform and AMP[6:1] decides the output stimulus voltage amplitude.



Amplitude signal AMP[6:1]	Stimulus current (Vst)
000100	2.0V
001000	4.0V
001100	6.0V
010000	8.0V
010100	10.0V

Fig. 3.3.3 Control signal and current level of 6-bits amplitude in voltage mode.

3.3.2 The Brief Illustration of Current-Mode Stimulation

Fig. 3.3.4 brief shows the real operation case, two channels are selected and respective output connect through the tissue, and the yellow region is the definition of one channel driver.

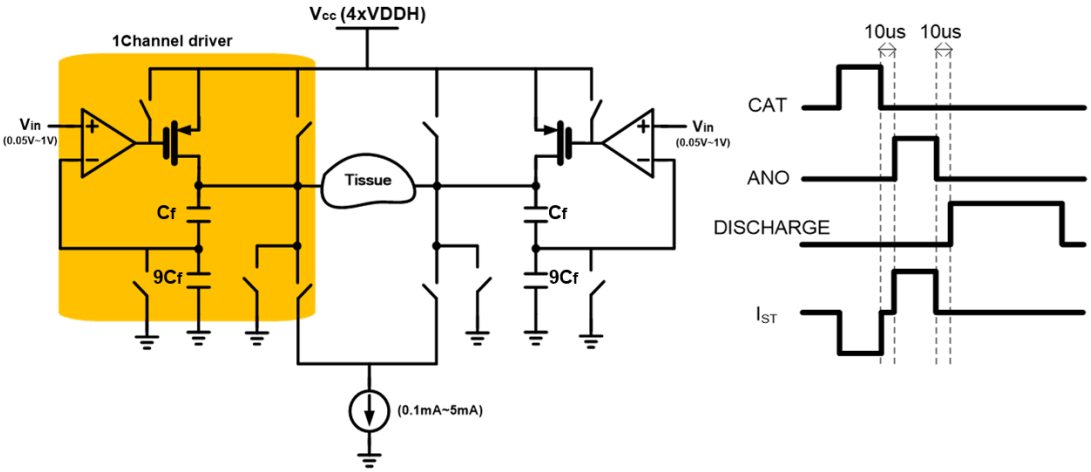


Fig. 3.3.4 The definition of one channel driver.

Fig. 3.3.5 illustrates cathode phase in current mode. First, the two PMOS in the figure are off-state, because these PMOS are used as output stage of op-amp in voltage mode and useless in current mode. Moreover, the upper right switch and the lower left switch are shorted, so the tissue is connected to highest voltage (Vcc) and current sink. Therefore it will cause cathode phase current go through the tissue and the current amplitude is decided by current sink below.

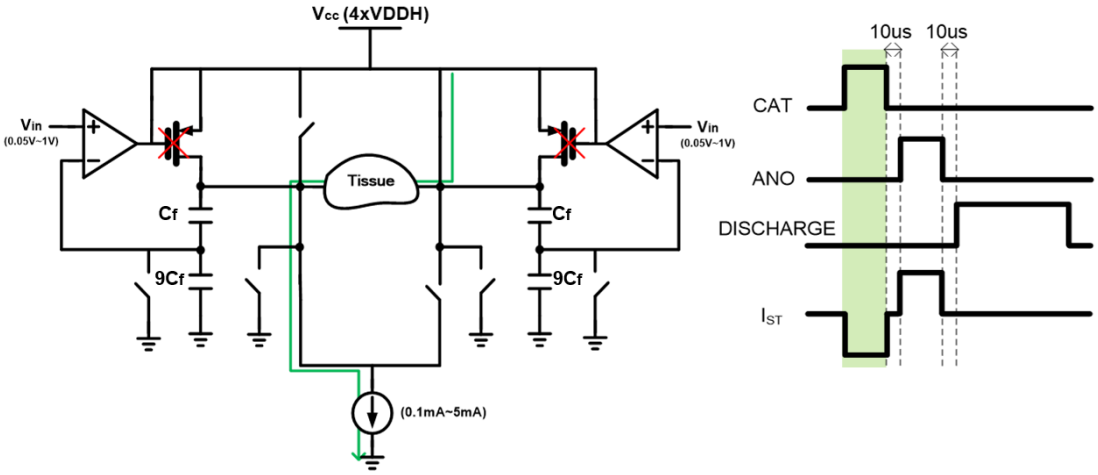


Fig. 3.3.5 The cathode phase in current mode.

As mentioned above, to avoid excessive positive and negative stimulation follow, the inter phase delay is needed. In this phase, the two PMOS in the figure are still off-state, and all of switches are open. So there will not cause any current flow through tissue, the value of stimulation current is equal to zero. The illustration is show in Fig. 3.3.6

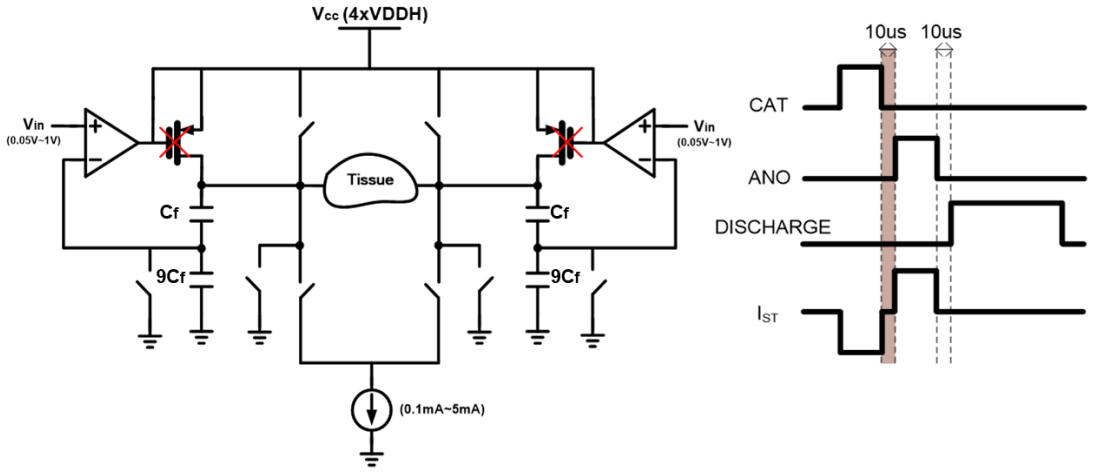


Fig. 3.3.6 The inter phase delay in current mode.

Fig. 3.3.7 illustrates anode phase in current mode. Just like cathode phase mentioned above, the two PMOS in the figure are still off-state, and the upper left switch and the lower right switch are shorted. In other words, the shorted switches in anode phase are contrast with cathode phase. So it will cause anode phase current go through the tissue.

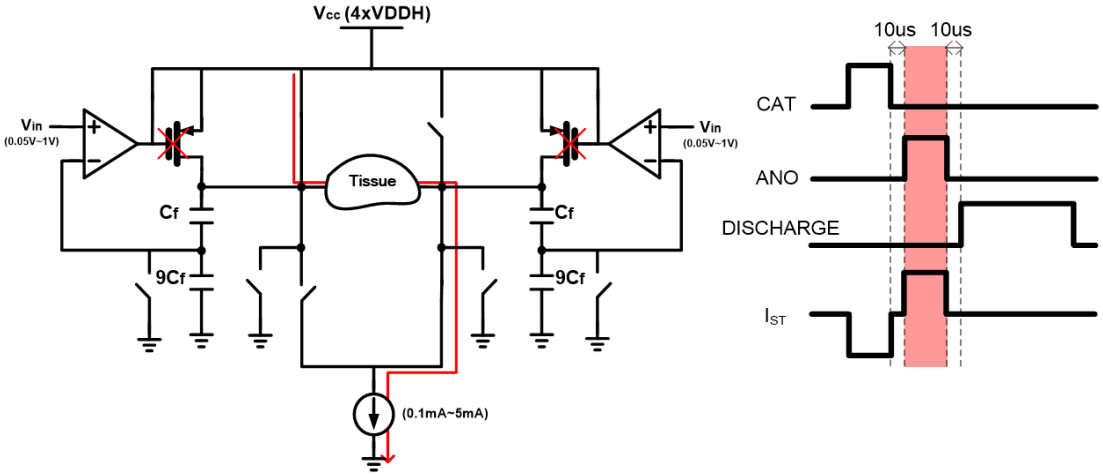


Fig. 3.3.7 The anode phase in current mode.

The last phase in current mode is the discharge phase. This purpose of this phase is to eliminate excess charge in the tissue due to mismatch between cathode phase and anode phase. In this phase, the four switches for cathode current and anode current are open, and the other two switches connected to ground are shorted. Thus the excess charge in the tissue can be discharged to ground.

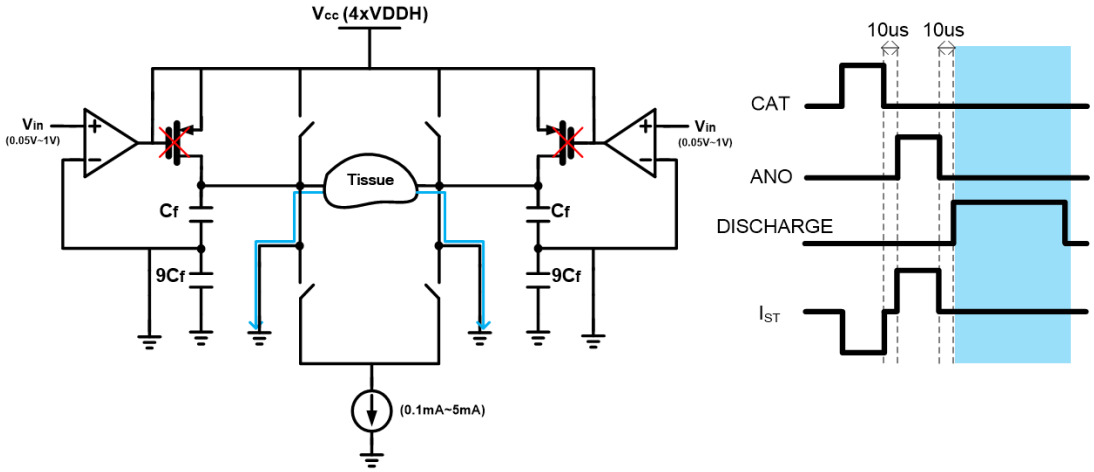


Fig. 3.3.8 The discharge phase in current mode.

3.3.3 The Brief Illustration of Voltage-Mode Stimulation

Fig. 3.3.9 shows the demonstration of voltage mode, two channels are selected and respective output connect through the tissue. The biggest difference with current mode is two PMOS will not always operate in off-state, because these PMOS are used as output stage of op-amp in voltage mode. Thus the two PMOS will be used to push the load (tissue) and reach target voltage.

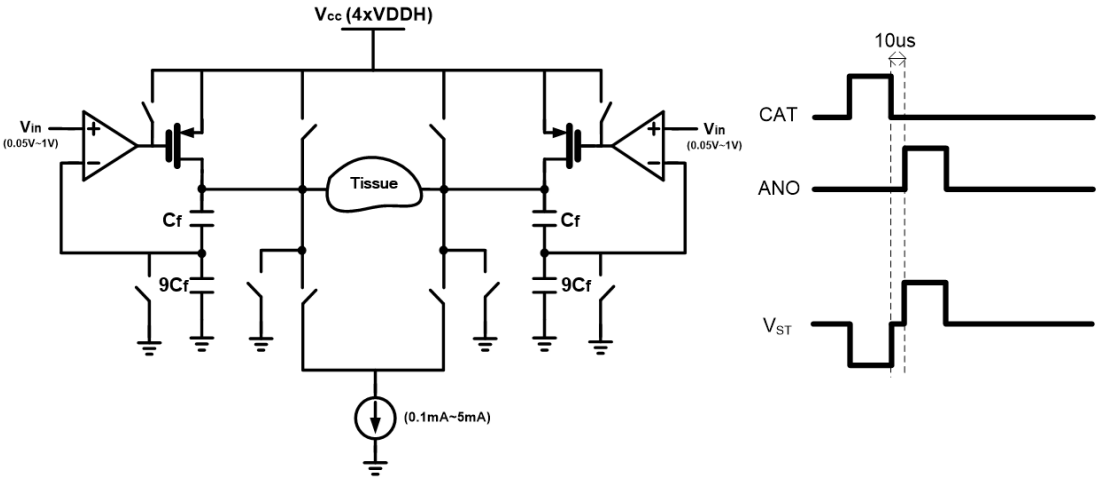


Fig. 3.3.9 The configuration of voltage mode.

Fig. 3.3.10 illustrates cathode phase in voltage mode. First, the right side PMOS in the figure is on-state, and the left side PMOS in the figure is off-state. Moreover, the left side of tissue is grounded and the node of capacitances is reset. The four switches for cathode current and anode current are open, and the amplitude of current sink is zero. Because the positive end of op-amp is connected to Vin, and the capacitances form a negative feedback system. Finally, 10Vin will push to right side of tissue. The 10Vin will be divided to Vin on negative end of right-side op-amp, thus ratio of capacitances is 1:9.

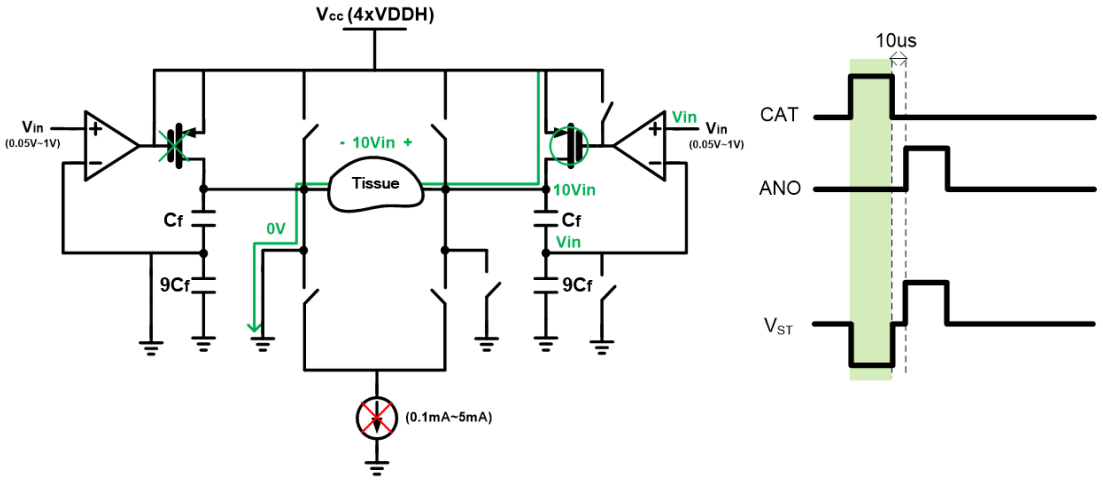


Fig. 3.3.10 The cathode phase in voltage mode.

As mentioned above, to avoid excessive positive and negative stimulation follow, the inter phase delay is needed. In this phase, the two PMOS in the figure are off-state. It is different with inter phase delay in current mode. In this phase, two sides of tissue are connected to ground and two nodes between capacitances are reset. So there will not cause any voltage difference on both sides of tissue, the value of stimulation voltage is equal to zero. The illustration is show in Fig. 3.3.11.

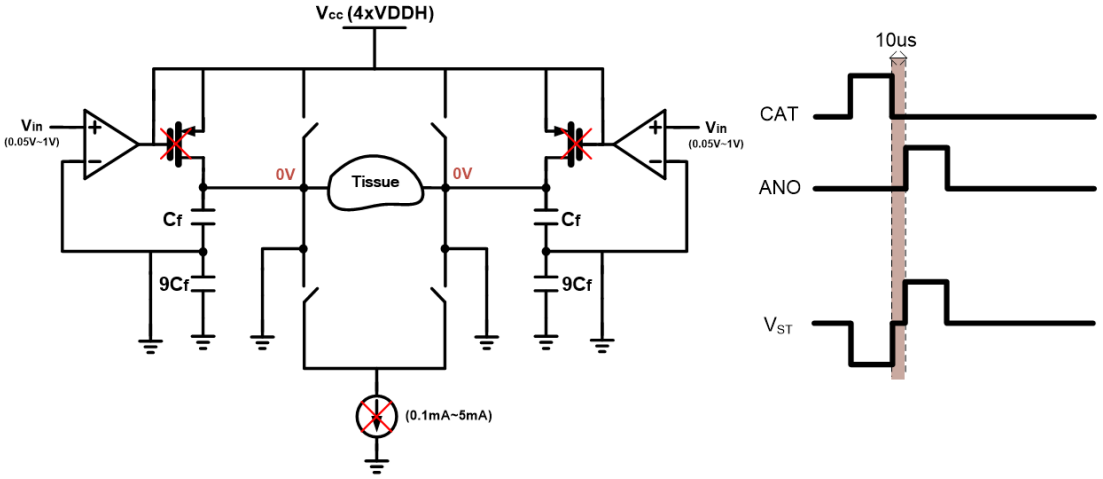


Fig. 3.3.11 The inter phase delay in voltage mode.

Fig. 3.3.12 illustrates anode phase in voltage mode. First, the left side PMOS in the figure is on-state, and the right side PMOS in the figure is off-state. Moreover, the right side of tissue is grounded and the node of capacitances is reset. The four switches for cathode current and anode current are open, and the amplitude of current sink is zero. Because the positive end of op-amp is connected to Vin, and the capacitances form a negative feedback system. Finally, 10Vin will push to left side of tissue. The 10Vin will be divided to Vin on negative end of left-side op-amp, thus ratio of capacitances is 1:9.

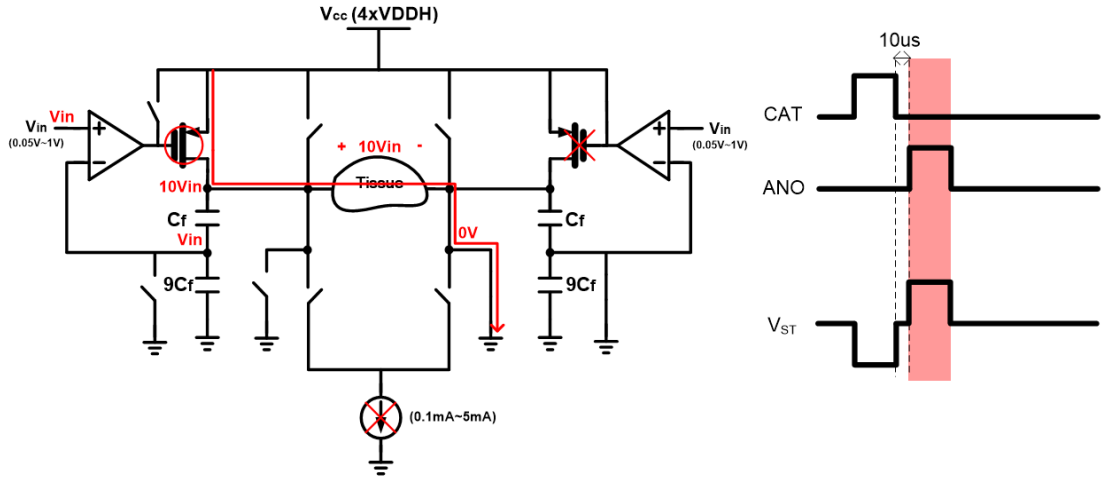


Fig. 3.3.12 The anode phase in voltage mode.

The last phase in voltage mode is the discharge phase. This purpose of this phase is to eliminate excess charge in the tissue due to mismatch between cathode phase and anode phase. Actually the discharge phase is the same as inter phase delay in voltage mode. In this phase, the two PMOS in the figure are off-state. It is different with inter phase delay in current mode. In this phase, two sides of tissue are connected to ground and two nodes between capacitances are reset. So there will not cause any voltage difference on both sides of tissue, the value of stimulation voltage is equal to zero. The illustration is show in Fig. 3.3.13

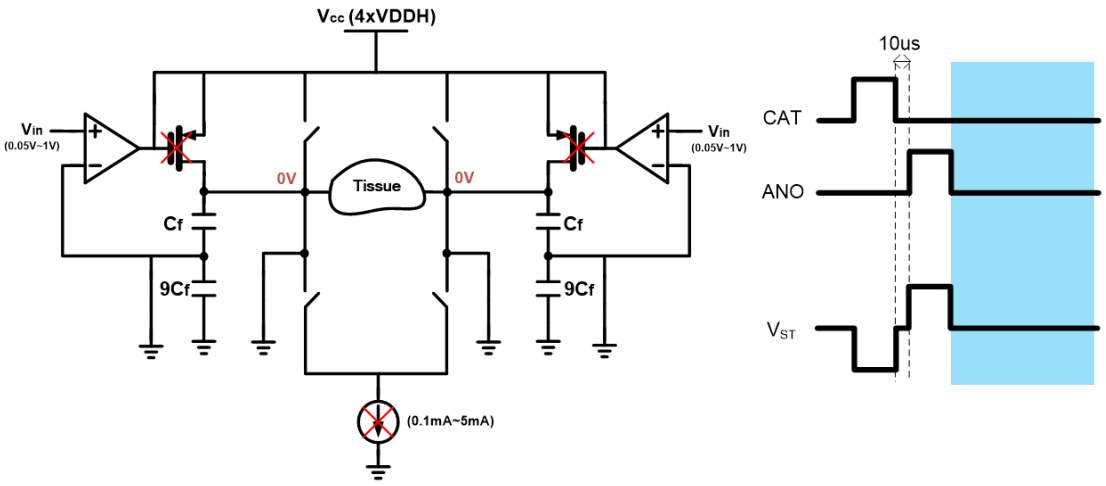


Fig. 3.3.13 The discharge phase in voltage mode.

3.3.4 The Driver Circuit

Fig. 3.3.14 shows the position of two channels driver in stimulator system. Since considering the real operation, it is easier to understand by explaining two channels simultaneously.

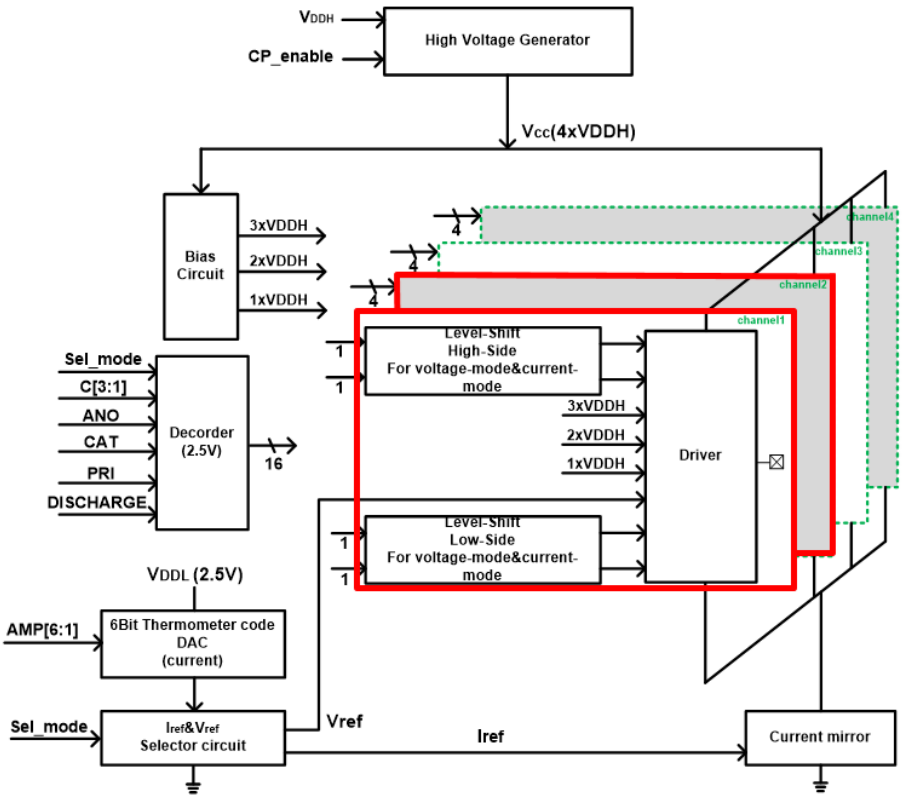


Fig. 3.3.14 The driver circuit in stimulator system.

The driver circuit of two channels is show in Fig. 3.3.15. As illustrated above, there are four switches (inside) for current mode use, and six switches (outer) for voltage mode use. The high voltage op-amp used in voltage mode also show in figure. All of these switches need to work with high-side level shift and low-side level shift in order to complete the proper operation in dual mode. Moreover, the driver circuit obviously work in high voltage region, so the 12V devices used in driver circuit. The highest voltage in driver circuit is about 18V~20V, thus the stack of MOS devices are needed. There are four stacked MOS in the figure, and the gate bias voltage of stacked MOS are 2xVDDH.

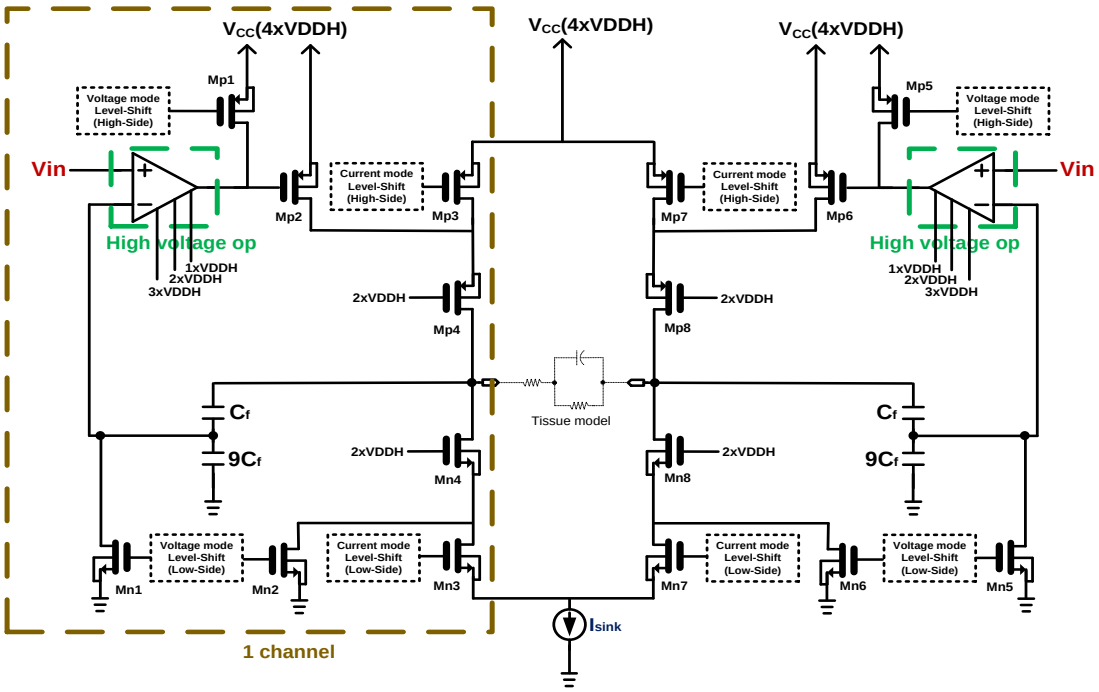


Fig. 3.3.15 The driver circuit of two channels example.

3.3.5 Voltage Limiting Technique

To prevent the devices from junction breakdown or gate oxide breakdown, we need ensure any two points voltage of all devices smaller than its limitation. Fig. 3.3.16 shows the concept of the voltage limiting technique [25]. Taking transistor Mn1 for an example, if there is no current (left side of Fig. 3.3.16) through Mn1, the source voltage of Mn1 will be charged up by leakage current until it is equal to its gate voltage. Otherwise, if there is a current flowing (right side of Fig. 3.3.16) through Mn1, the aspect ratio of the transistor is designed to be large enough so that the V_{GS} of Mn1 are slightly larger than the threshold voltage (V_{th}). The drain voltage of Mn1 is controlled by the source voltage of the transistor cascaded above. The body node of every transistor is connected to its own source node to prevent large voltage leading gate oxide breakdown so that the deep N-well layer is used to isolate the P-well region of each stacked NMOS from the common P-substrate. The structure of PMOS works in a

similar way. Following this technique, when the gate voltages of all transistors are carefully determined, the transistors will not overstress in high voltage condition and have more reliability.

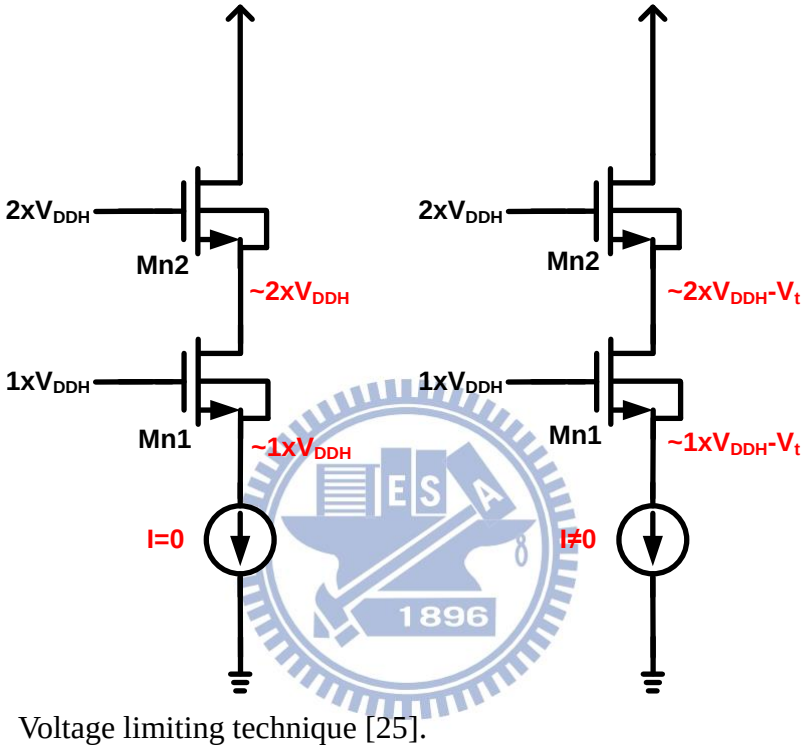


Fig. 3.3.16 Voltage limiting technique [25].

3.3.6 High Voltage Op-amp

The high voltage op-amp is used to push loading in voltage mode. The op-amp use folded cascade architecture [26], because this structure is more suitable for low voltage region and high voltage region simultaneous existence. In Fig. 3.3.17, the left part of op-amp is low voltage operating region, this part contains constant gm circuit, start-up circuit. Constant gm circuit can generate current source [27], and the current source is decided by the size of Mn3, Mn4 and value of R. But there is a certain probability that constant gm circuit will not work correctly. When the power on, the gate voltage of

PMOS is high voltage and the gate voltage of NMOS is low voltage due to parasitic capacitance. If this situation happen, the constant gm circuit cannot produce any current, in other words, the current is zero. Thus constant gm circuit need to add the start-up circuit. When the mentioned situation happen, start-up circuit will pull down the gate voltage of PMOS and pull up the gate voltage of NMOS to avoid zero current situation.

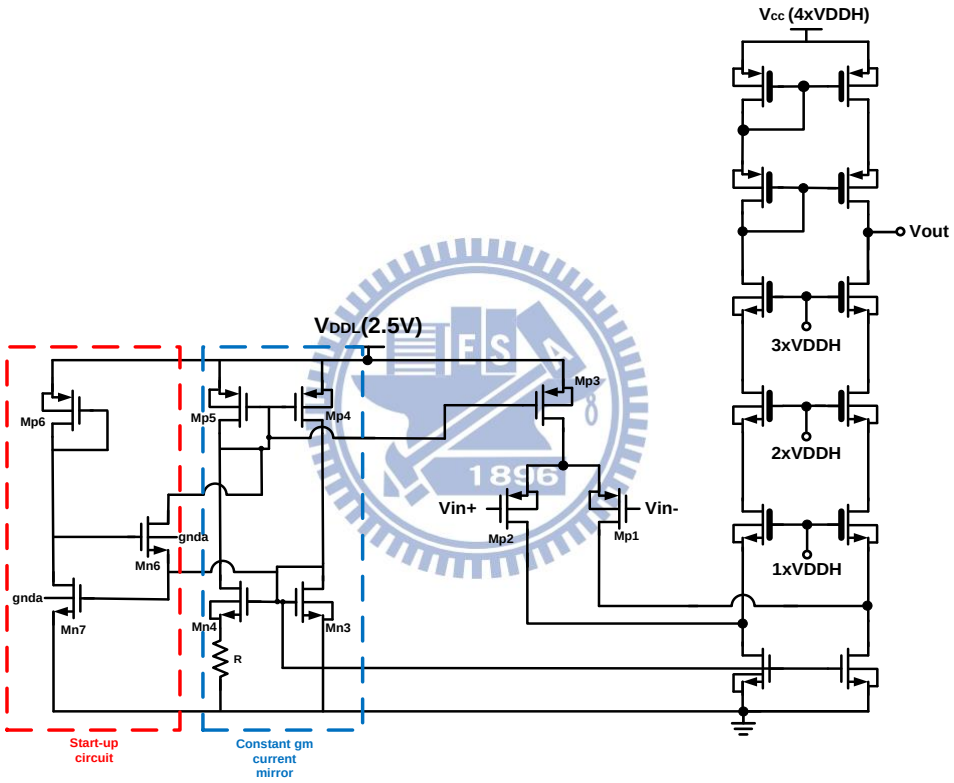


Fig. 3.3.17 The high voltage op-amp.

3.3.7 The 6-bits Thermometer Code DAC

The 6-bits thermometer code DAC play a current source role in overall system. As we can see in Fig. 3.3.18, the current source is decided by bandgap reference and Rref. In this case, the bandgap reference will generate 1V voltage and the Rref is 100kΩ, so the unit current source is 10μA. The DAC is 6-bits, thus the output current is

10μA~630μA. Thermometer code DAC has advantage compared to traditional type DAC [28]. First, all the size of MOS is the same, this will make advantage of layout matching. The match considerations in current mirror is most important. Second, if the operation is ramp case, the thermometer code always turn on or turn off one switch in one timing, this operation will reduce the current glitch. Moreover, the application of ramp case is using for Parkinson's disease.

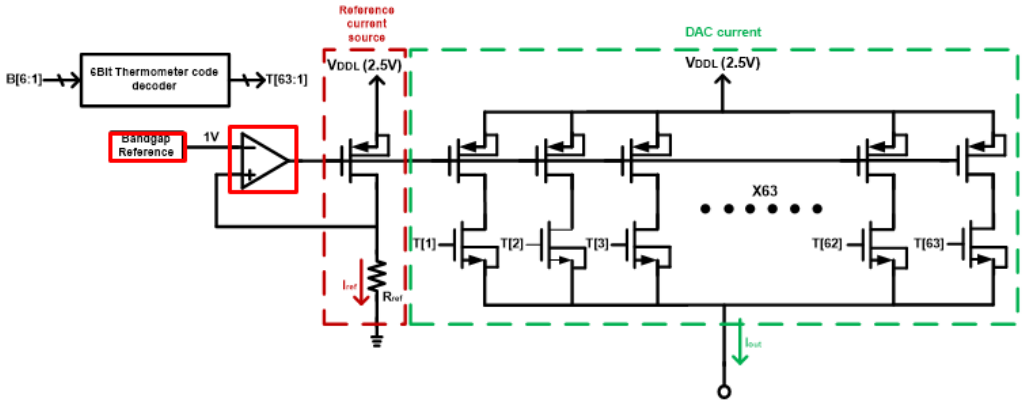


Fig. 3.3.18 The 6-bits thermometer code DAC.

3.3.8 The Sub-1V Bandgap Reference

The sub-1V bandgap reference [29] is show in Fig. 3.3.19. The bandgap reference voltage is decided by R1, R2, R3 and ratio of diode. The output voltage formula is show in (3.1), the term of V_{be} has negative temperature coefficient and the term of V_T has positive temperature coefficient. So control the ratio of two term, that is, R1, R2 and ratio of diode, can make zero temperature coefficient point. Considering the real application is implantable, so the operating temperature of the chip is about 37℃ (body temperature). The zero temperature coefficient point should be designed at 37℃, and

the pre-layout simulation result is 1.0016V and post-layout simulation result is 1.00175V are show in right side of Fig. 3.3.19.

$$V_{out} = \left(\frac{V_{be1}}{R_1} + \frac{V_T \ln(N)}{R_2} \right) \times R_3 \tag{3.1}$$

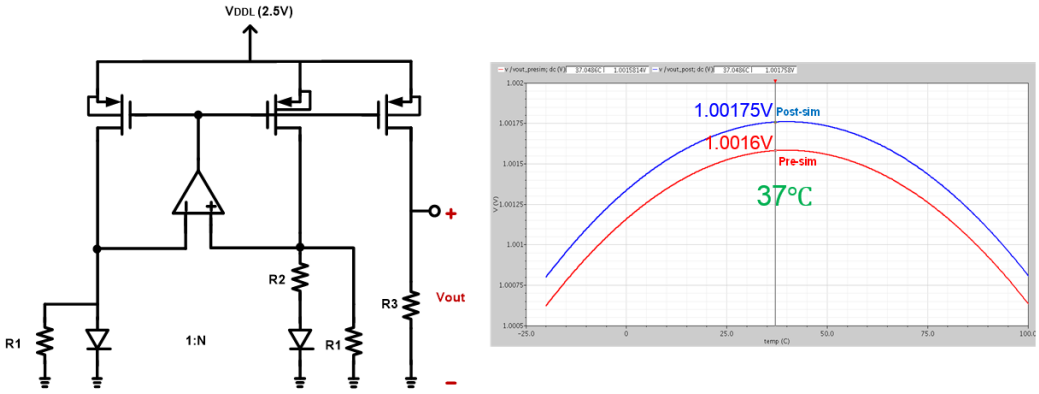


Fig. 3.3.19 The sub-1V bandgap reference circuit.

3.3.9 The Two Stage CMOS Op-amp

The two stage CMOS op-amp used in stimulator system is show in Fig. 3.3.20. Just like high voltage op-amp, the two stage CMOS op-amp includes constant gm circuit to generate current source and start-up circuit to avoid problem of zero current.

Because the structure is two stage, there will be two poles appear in the two stage CMOS op-amp. Thus frequency compensation is needed, as show in figure, the method of RC compensation is applied. The first stage of op-amp is PMOS differentia pair (Mp1 and Mp2), and it can amplify input signal and turn signal from differential-end to single-end. Mn1 and Mn2 used as active load. The second stage of op-amp is a common source configuration amplifier (Mn8). Similarly, Mp7 used as active load.

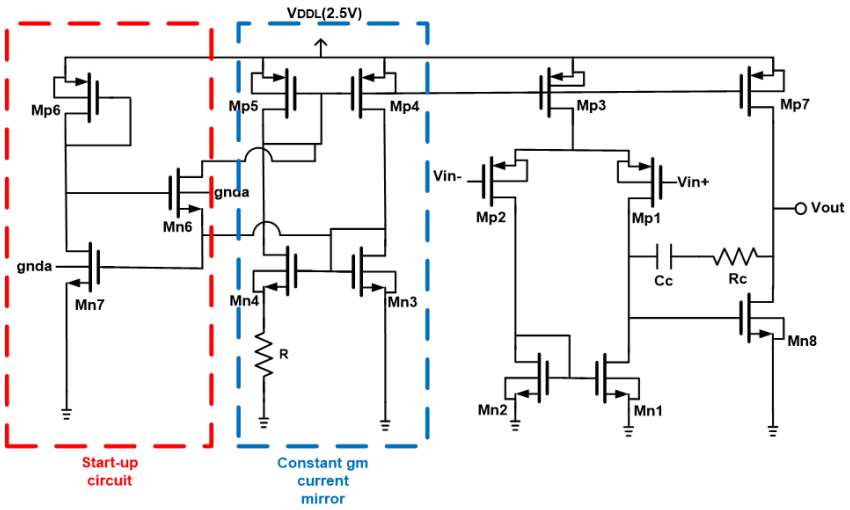
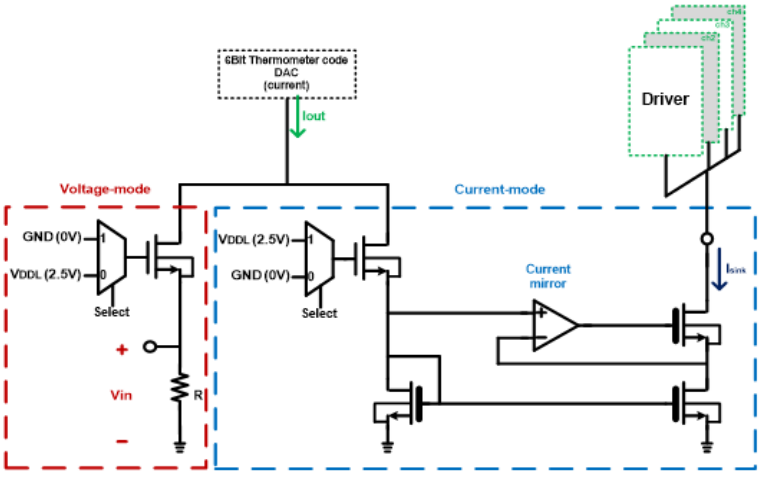


Fig. 3.3.20 The two stage CMOS op-amp used in stimulator system.

3.3.10 The Mode Select Circuit and Current Mirror

As mentioned above, the current source of current mode and voltage mode is the same, and the current source is generated by 6-bits thermometer code DAC. When we get current source, there must be some circuit to select current signal or voltage mode.

The mode select circuit is show in Fig. 3.3.20. We used two MUXs to decide which mode now is. And the mode select truth table is show in figure. The current mode signal use current source and current mirror to produce expected output current and the voltage mode signal use current source and a resistance to produce.

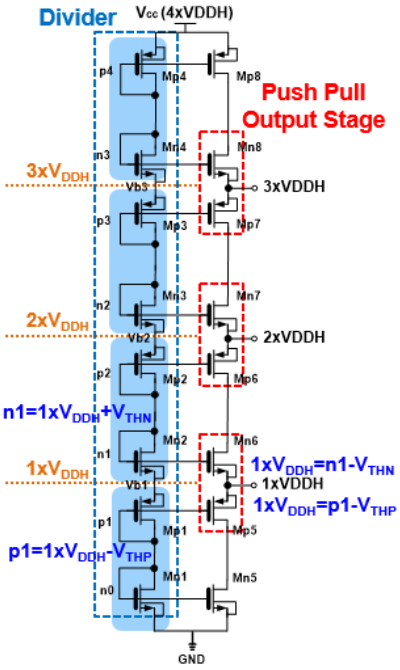


Select	Function
V_{DDL}(2.5V)	Current mode
GND(0V)	Voltage mode

Fig. 3.3.21 The mode select circuit and current mirror.

3.3.11 Reference Voltage Generator

Fig. 3.3.22 shows the schematic of the reference voltage generator. All the transistors in bias circuit are 5V I/O devices. This circuit divides Vcc ($4xV_{DDH}$) into 3 levels ($1xV_{DDH}$, $2xV_{DDH}$, and $3xV_{DDH}$) to provide the expected reference voltages for the stimulus unit. Transistors M_{N1}~M_{N4}, M_{P1}~M_{P4} perform the function of the voltage divider, and transistors M_{N5}~M_{N8}, M_{P6}~M_{P8} perform the function of the push pull output stage. Because the size of transistors are the same, the level of V_{b1}, V_{b2}, V_{b3} will be $1xV_{DDH}$, $2xV_{DDH}$, $3xV_{DDH}$. The gate voltage of M_{P1} (V_{p1}) is $1xV_{DD}$-V_{thp} and the gate voltage of M_{N2} (V_{n1}) is $1xV_{DD}$+V_{thn}. Thus, the lowest output node decided by transistors M_{P1} and M_{N1} is $1xV_{DD}$. For the same principle, the second output node is $2xV_{DD}$ and third output node is $3xV_{DD}$. And the right side of Fig. 3.3.22 shows the three nodes output voltage in five different process corners. Output voltage of all corners are the same, this proves the circuit can tolerate process variation.



	$1xV_{DDH}$	$2xV_{DDH}$	$3xV_{DDH}$	$4xV_{DDH}$
FF	4.5	9	13.5	18
FS	4.5	9	13.5	18
TT	4.5	9	13.5	18
SF	4.5	9	13.5	18
SS	4.5	9	13.5	18

Fig. 3.3.22 Reference voltage generator.

3.3.12 Level-Shift

Fig. 3.3.23 shows the schematic of the level shift. Initially, the gate voltage of Mn1 is 0V, the gate voltage of Mn2 is 2.5V (V_{DDL}) due to inverter (core device). So Mn1 is off-state and Mn2 is on-state. Because the previous state, the gate voltage of Mp2 is 0V, that is, Mp2 is on-state too. So the pull-down current of Mn2 must bigger than pull-down current of Mp2. Otherwise, the level-shift will not turn state. So the key point of design concept is that the size of transistors Mn1 and Mn2 must be larger than Mp1 and Mp2. If design properly, the drain voltage of Mn2 will be pulled-down to 0V. Then Mp1 will be turned on and the drain voltage of Mp1 will up to 5V (V_{DDH}). Finally, the Mp2 will be fully turned off, so the drain voltage of Mp2 is 0V and the output voltage is 5V (V_{DDH}) due to inverter (I/O device).

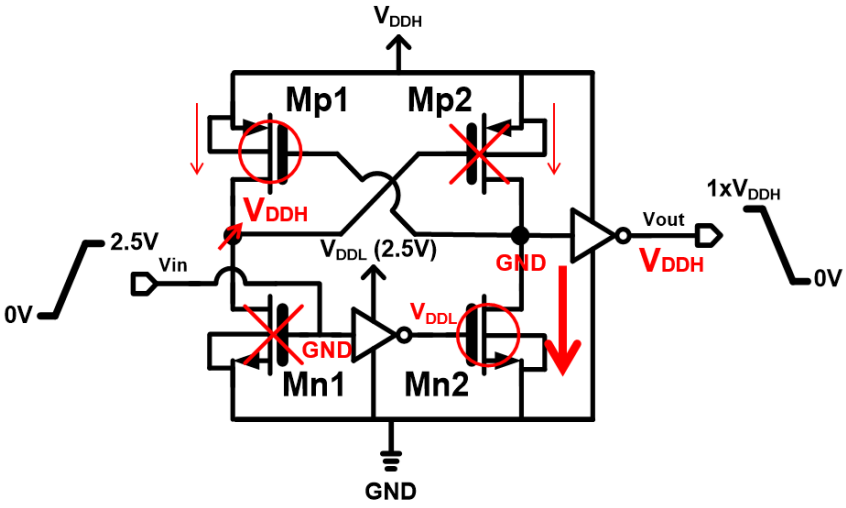


Fig. 3.3.23 Level-shift schematic.

3.4 Simulation and Measurement Results

3.4.1 Simulation Results

This case shows operation in current mode. Fig. 3.4.1 shows the simulation result of the biphasic stimulus current (I_{ST}) at different amplitude (all scale stimulus current) and the 12V HV devices overstressed test shows voltage between drain, source, gate and bulk of all the transistors in stimulus driver. The simulation result observes that the driver is not overstressed in steady state but has maximum voltage which is 11.15V in transient state. The proposed stimulator had been implemented in 0.25-μm HV USG 2.5/5/12V process.

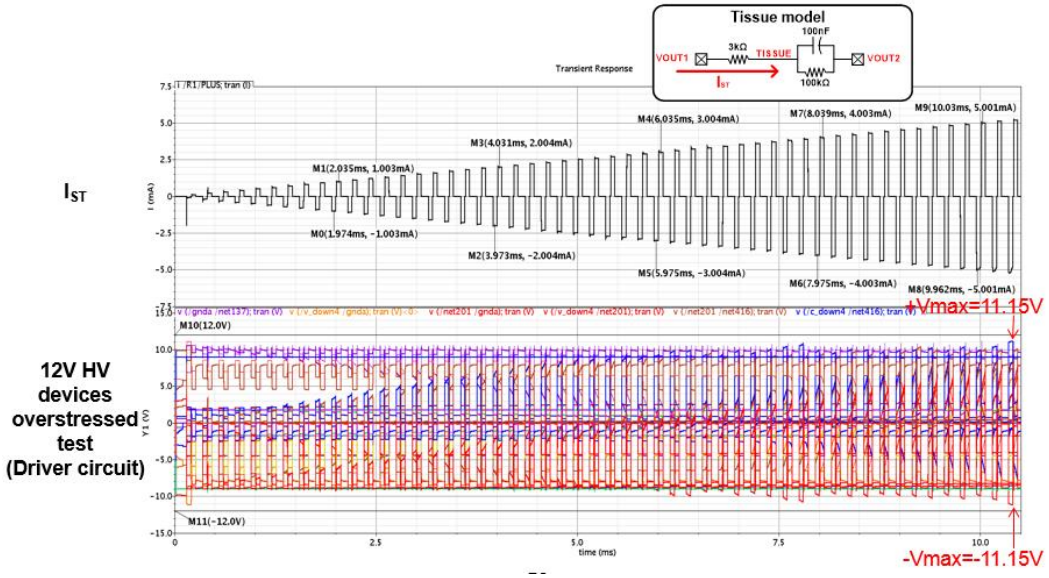


Fig. 3.4.1 The simulation result of all scale stimulus current.

This case shows operation in voltage mode. Fig. 3.4.2 shows the simulation result of the biphasic stimulus voltage (V_{ST}) at different amplitude (all scale stimulus voltage) and the 12V HV devices overstressed test shows voltage between drain, source, gate and bulk of all the transistors in stimulus driver. The simulation result observes that the driver is not overstressed in steady state but has maximum voltage which is 10.71V in transient state.

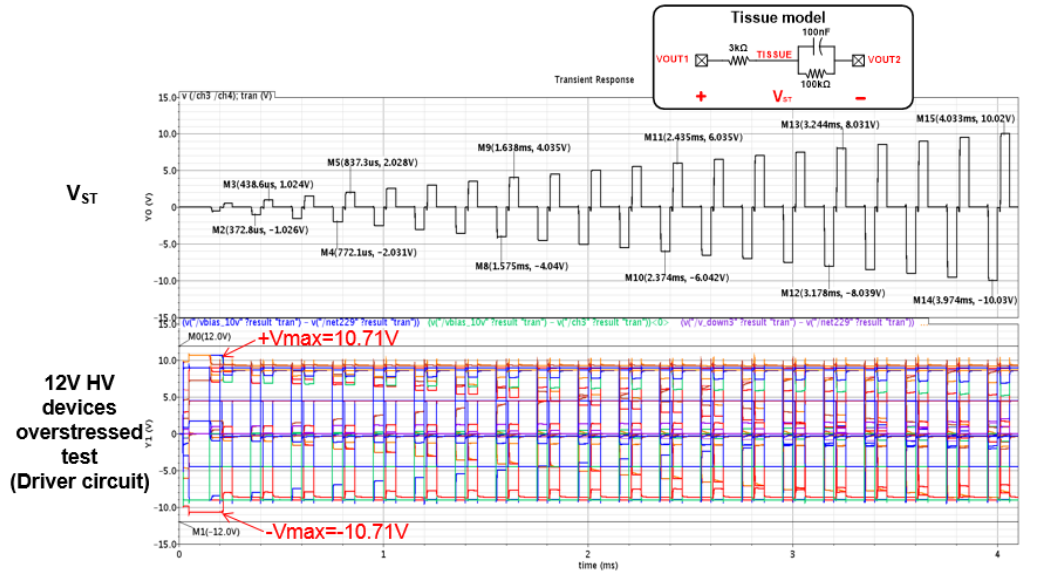


Fig. 3.4.2 The simulation result of all scale stimulus voltage.

To verify the stimulus driver will not have overstressed problem when another pair of drivers are not active (chosen) to simulate real application case. Fig. 3.4.3 shows the simulation result of the stimulus driver by applying a pulse signal to output and the Mp3 and Mn3 are off-state and the figure of 12V HV devices overstressed test shows voltage between drain, source, gate and bulk of all the transistors in driver. The result waveform proves that all the transistors in driver will not be overstressed (±12V).

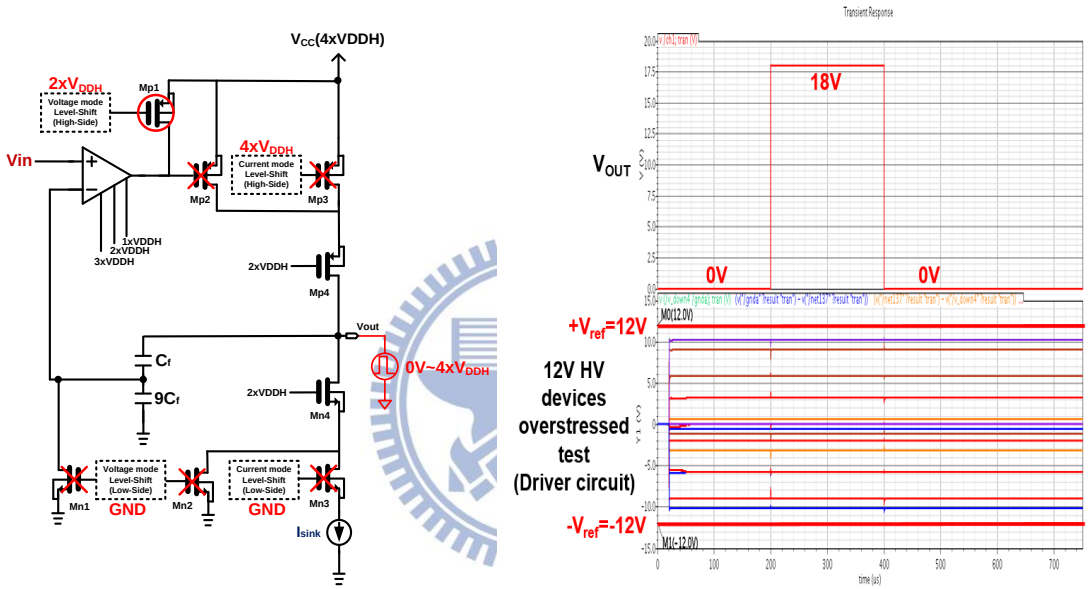


Fig. 3.4.3 Overstress test of driver by applying a pulse signal on driver output.

Initially, two channel drivers are chosen to simulate real application case. Fig. 3.4.4 shows the simulation result of two channel drivers at power on state. The figure of 12V HV devices overstressed test shows voltage between drain, source, gate and bulk of all the transistors in two channel drivers. The result waveform proves that all the transistors in drivers will not be overstressed (±12V).

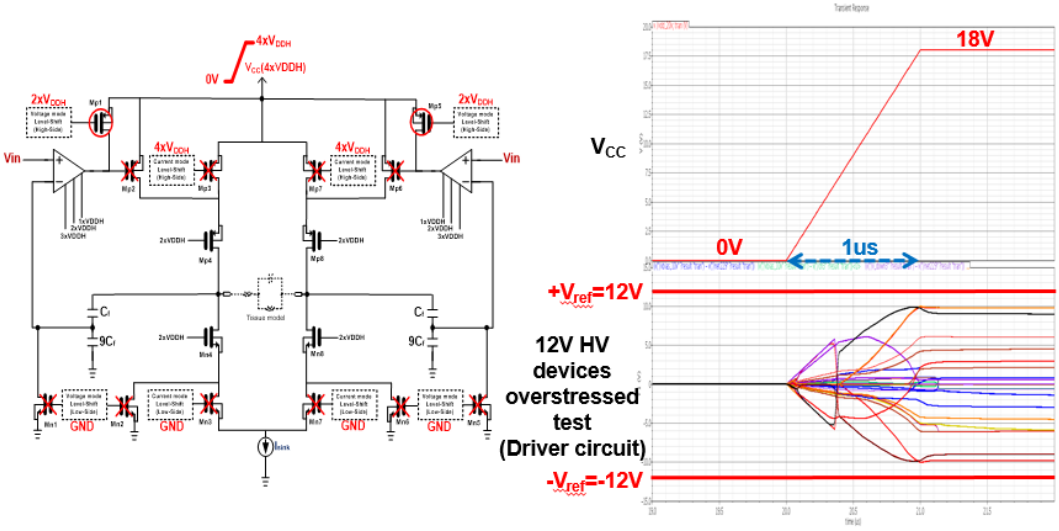


Fig. 3.4.4 Overstress test of two channel drivers at the power on state.

3.4.2 Measurement Results

The layout consists of some sub-blocks, including level-shift (high-side), level-shift (low-side), stimulus drivers, bias circuit, 6-bits thermometer code DAC, current mode & voltage mode select circuit, current mirror, decoder, and high voltage generator is shown in Fig. 3.4.5. The total area is 2.139 × 2.491 mm^2. The proposed stimulator system had been implemented in 0.25-μm HV USG 2.5/5/12V process.

And the microphotograph of the fabricated chip is shown in Fig. 3.4.6. The block of microphotograph is same as the layout.

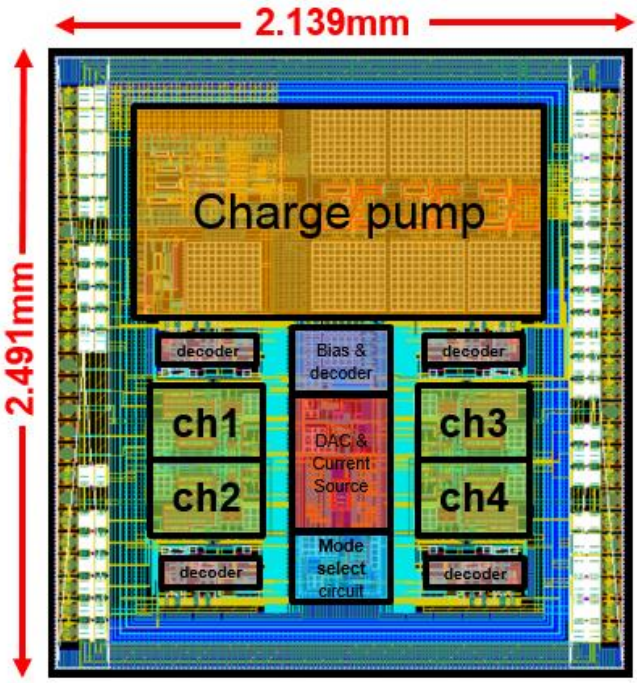


Fig. 3.4.5 The layout of the fabricated stimulator chip.

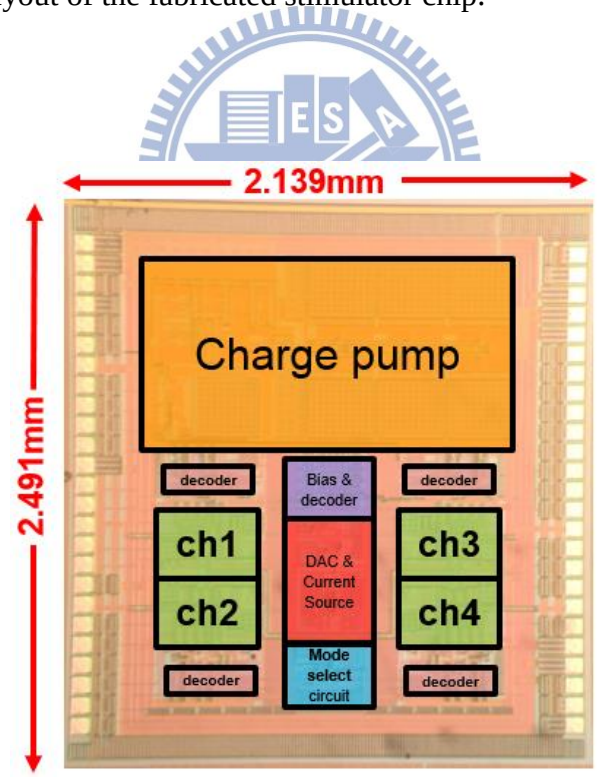
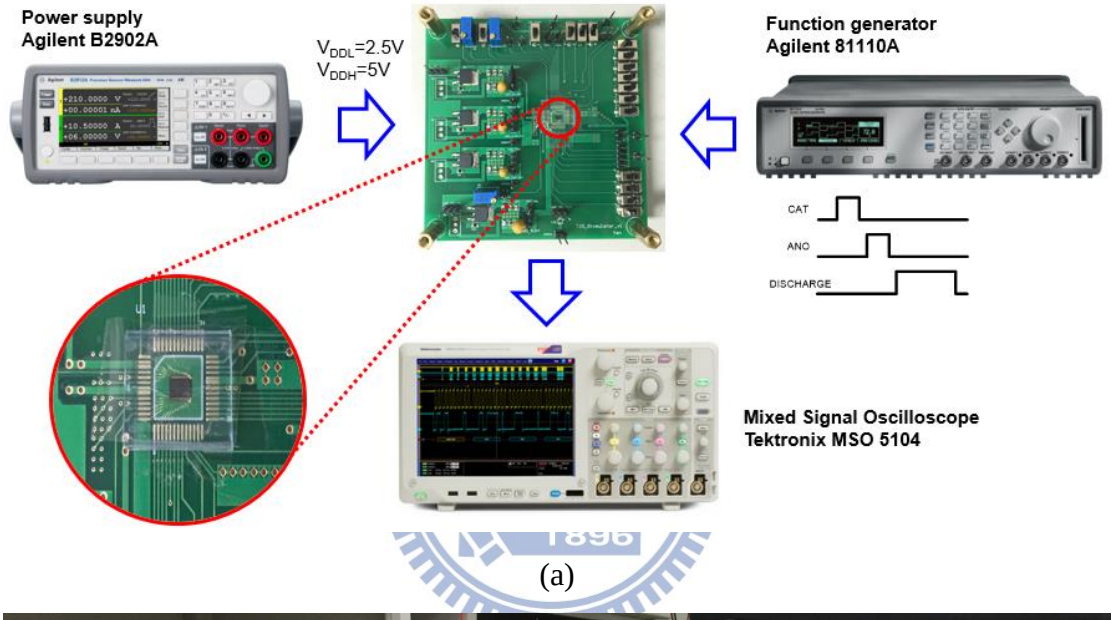
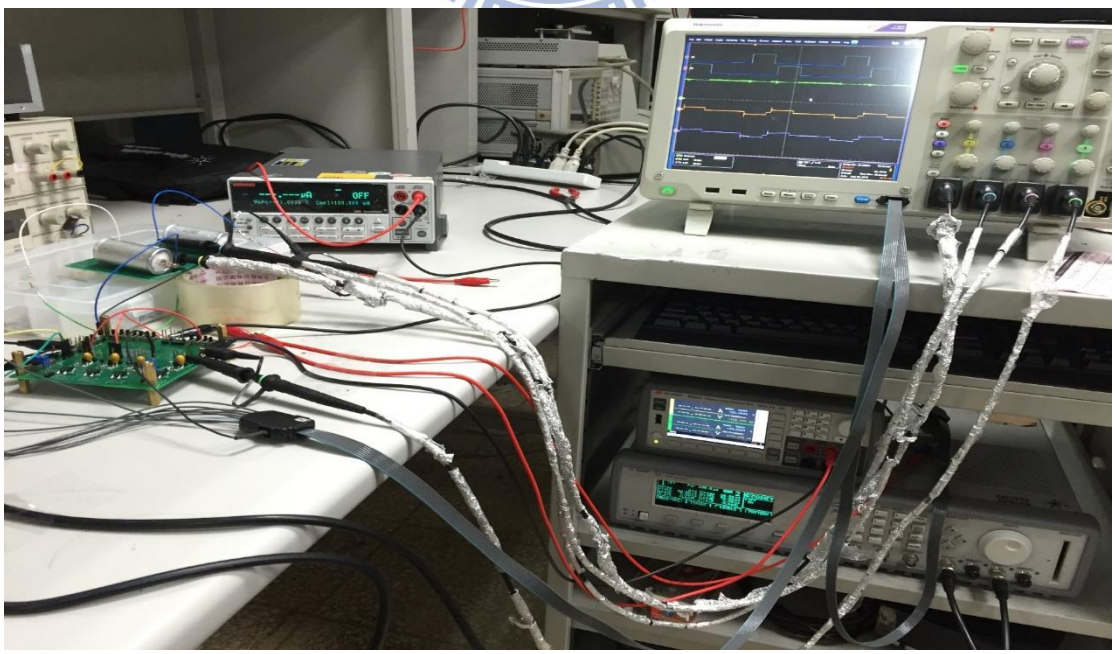


Fig. 3.4.6 The microphotograph of the fabricated stimulator chip.

Fig. 3.4.7(a) shows the measurement setup of stimulator driver. Agilent B2902A (power supply) is used to provide the fixed voltage 2.5V (V_{DDL}) and 5.0V (V_{DDH}). Agilent 8110A (function generator) is used to provide control signals CAT, ANO, and DISCHARGE. Tektronix MSO 5104 (oscilloscope) is used to observe the output waveforms of the stimulator system. The real measurement environment is shown in Fig. 3.4.7(b).



(a)



(b)

Fig. 3.4.7 The measurement setup of driver (a). Real measurement environment (b).

Operating in current mode, and the 6-bit amplitude signal is set to logic 000100 (1mA), the pulse width of CAT and ANO signals are 50μs, the interphase delay between ANO/CATH 10μs, the output current waveform is showed in Fig. 3.4.8. The tissue model of this condition: R_S, C_{dl}, and R_f value are 3kΩ, 100nF, and 100kΩ. The waveform shows I_{st} (current flows through Rs), V_{st} (voltage across whole tissue model) and V_{CC} (high voltage generator output).

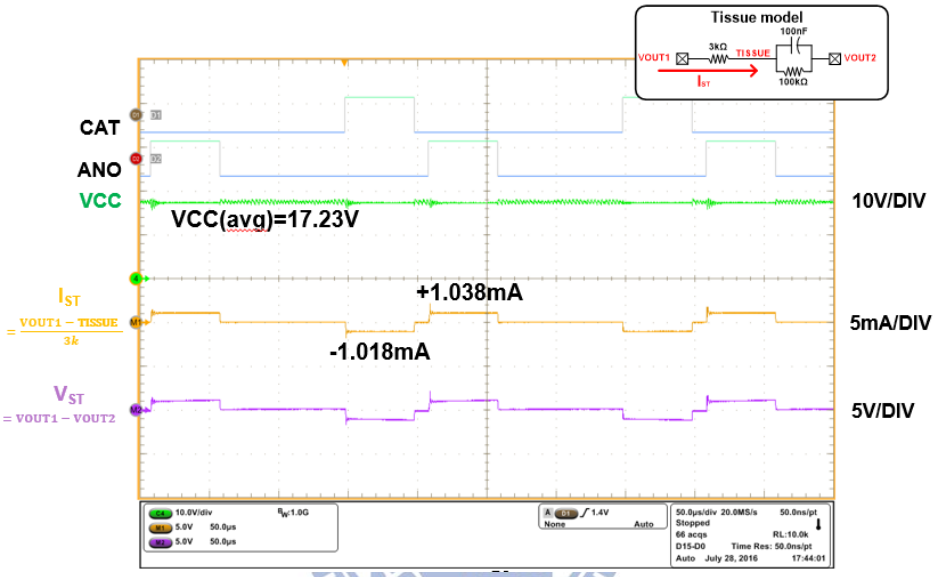


Fig. 3.4.8 The measurement result of current mode at output current=1mA.

Fig. 3.4.9 shows the case of current mode in output current 3mA, other measurement setup and parameter are the same as mentioned above.

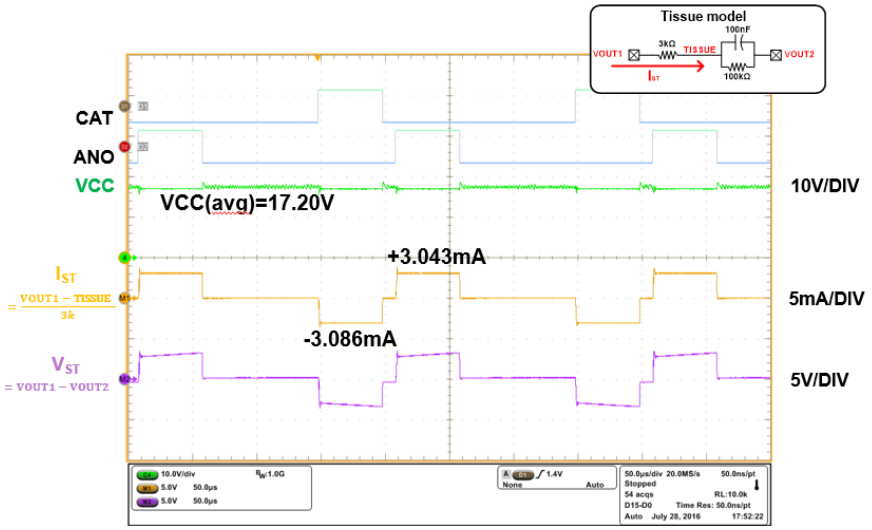


Fig. 3.4.9 The measurement result of current mode at output current=3mA.

Fig. 3.4.9 shows the case of current mode in output current 5mA, other measurement setup and parameter are the same as mentioned above.

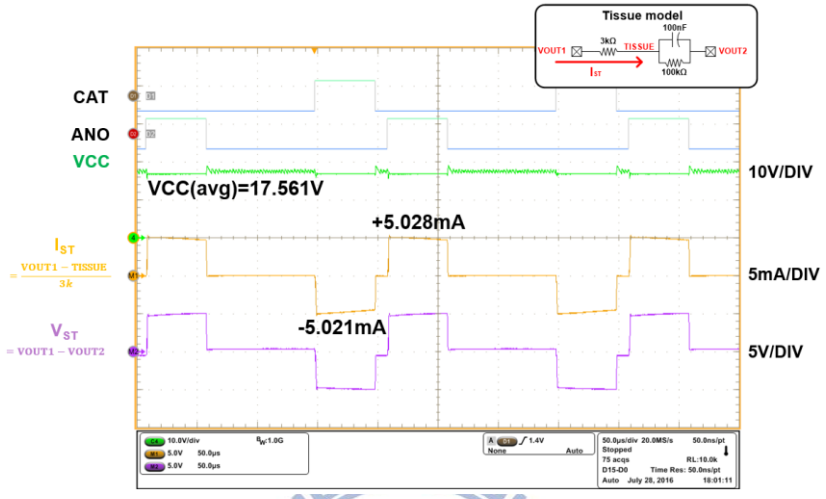


Fig. 3.4.10 The measurement result of current mode at output current=5mA.

The result of all current level is show Fig. 3.4.11. In case of Rs=3kΩ, because the highest voltage (Vcc) is not high enough (about 17.5V), the headroom of current sink is suppressed. So the 5mA current waveform is distorted. But 4mA current waveform is normal. And the stimulation current is as expected in case of Rs=1kΩ.

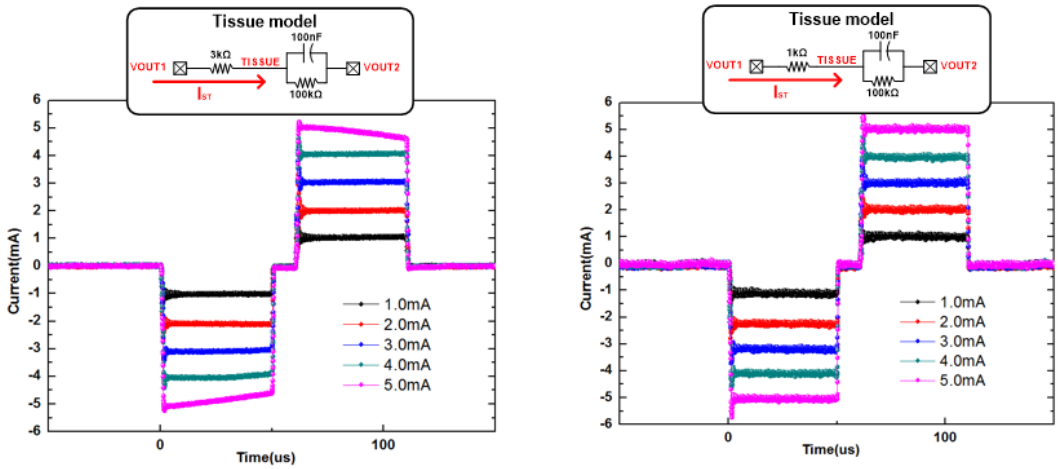


Fig. 3.4.11 The measurement result of all current levels in Rs=1k and Rs=3k.

Operating in voltage mode, and the 6-bit amplitude signal is set to logic 000100 (2V), the pulse width of CAT and ANO signals are 50μs, the interphase delay between ANO/CATH 10μs, the output current waveform is showed in Fig. 3.4.12. The tissue model of this condition: R_S, C_{dl}, and R_f value are 3kΩ, 100nF, and 100kΩ. The waveform shows V_{st} (voltage across whole tissue model), I_{st} (current flows through Rs), and V_{CC} (high voltage generator output).

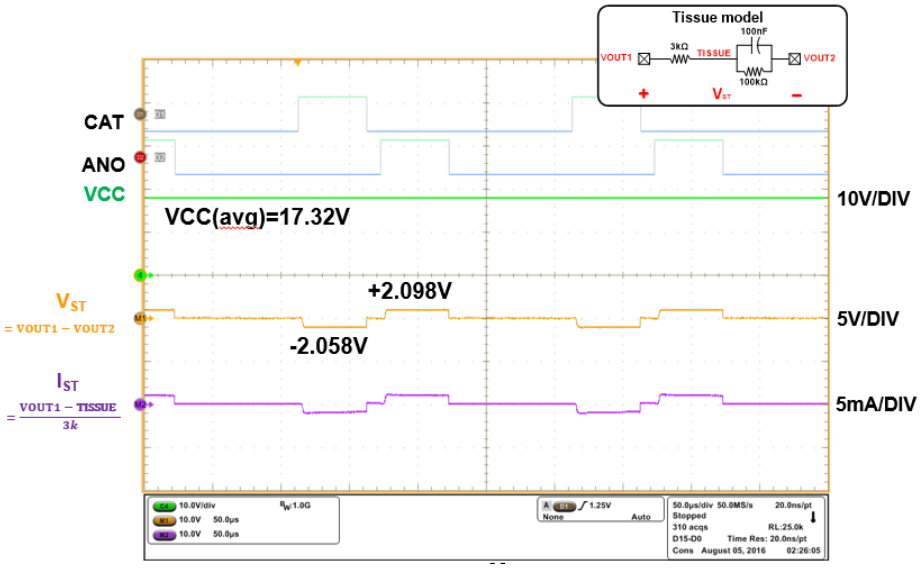


Fig. 3.4.12 The measurement result of voltage mode at output voltage=2V.

Fig. 3.4.13 shows the case of voltage mode in output voltage 2V, other measurement setup and parameter are the same as mentioned above.

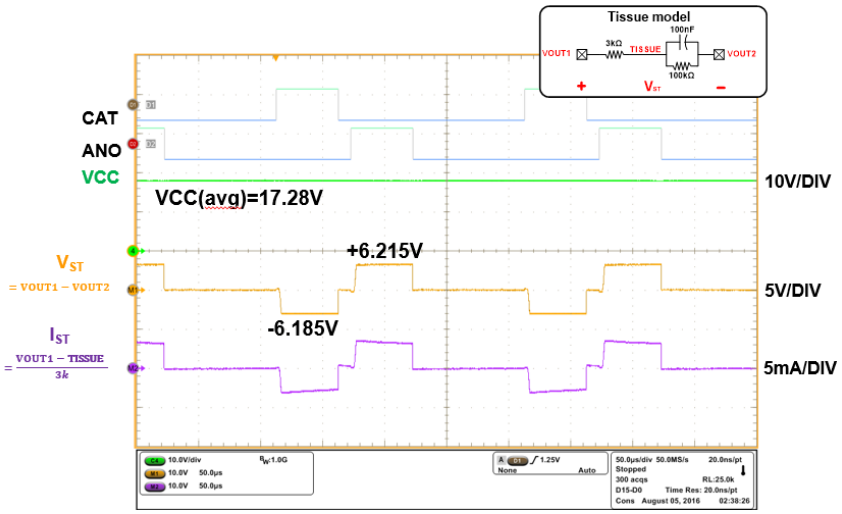


Fig. 3.4.13 The measurement result of voltage mode at output voltage=6V.

Fig. 3.4.14 shows the case of voltage mode in output voltage 10V, other measurement setup and parameter are the same as mentioned above.

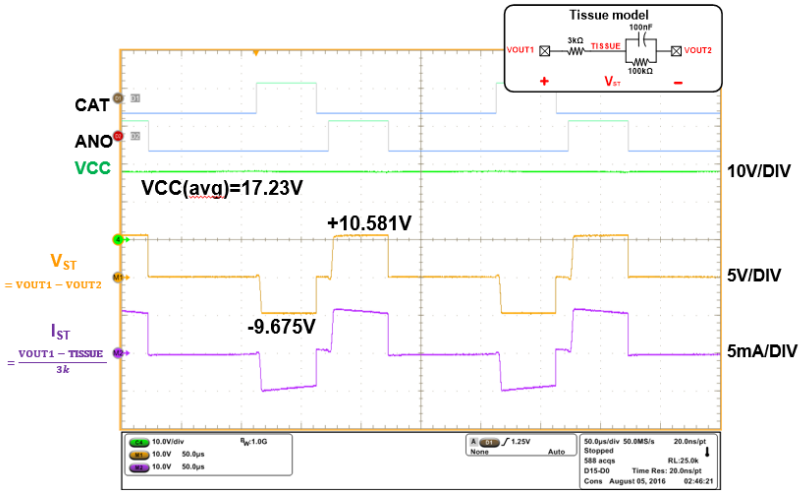


Fig. 3.4.14 The measurement result of voltage mode at output voltage=10V.

The result of all voltage level is show Fig. 3.4.15. The waveforms of case Rs=3kΩ and the case Rs=1kΩ are as expected.

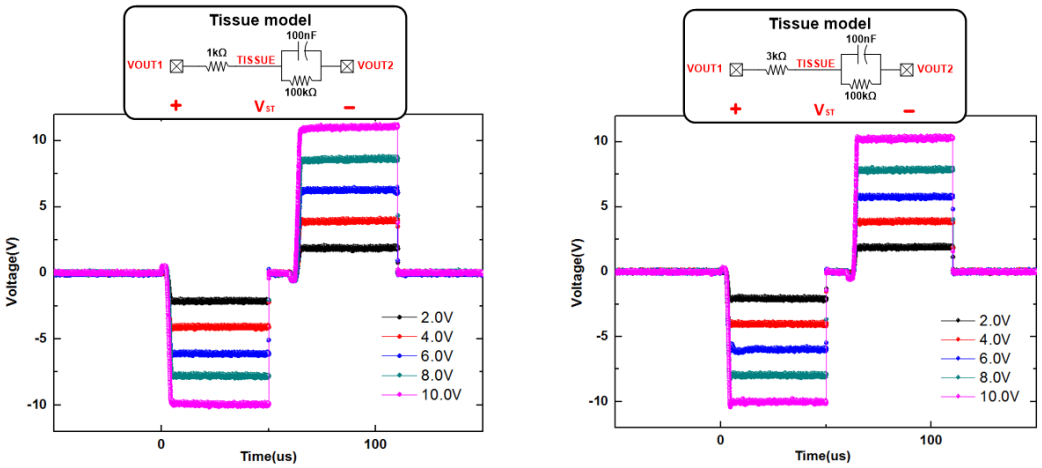


Fig. 3.4.15 The measurement result of all voltage levels in Rs=1k and Rs=3k.

Table 3.4 summarizes the stimulus driver specifications, as we can see, although there are mismatch in current/voltage amplitude, the current mode and voltage mode function exist in the same chip simultaneously is realized.

Table 3.4

Summary of stimulus driver specifications.

	Spec.	Pre-layout simulation	Post-layout simulation	Measurement
V_{DDL} (V)		2.5V		
Stimulus Current Amplitude (mA)	+1.000, -1.000, +2.000, -2.000, +3.000, -3.000, +4.000, -4.000, +5.000, -5.000,	+1.004, -1.004, +2.006, -2.006, +3.008, -3.008, +4.008, -4.008, +5.008, -5.008,	+1.004, -1.004, +2.005, -2.006, +3.008, -3.008, +4.008, -4.009, +5.007, -5.008,	+0.983, -0.999, +1.994, -2.002, +2.996, -3.003, +3.999, -4.002, +5.002, -5.005,
Cathodic / Anodic Current Matching	minimum	0.0341%	0.156%	1.21%
Stimulus Voltage Amplitude (V)	+2.000, -2.000, +4.000, -4.000, +6.000, -6.000, +8.000, -8.000, +10.00, -10.00,	+2.028, -2.031, +4.035, -4.040, +6.035, -6.042, +8.031, -8.039, +10.02, -10.03,	+2.029, -2.036, +4.032, -4.048, +6.031, -6.050, +8.028, -8.048, +10.01, -10.04,	+1.995, -2.021, +4.020, -4.059, +6.038, -6.095, +8.005, -8.021, +10.10, -9.92,
Cathodic / Anodic Voltage Matching	minimum	0.15%	0.86%	2.96%
Standby Power (W)	minimum	141uW	186uW	298uW
Process	0.25-μm HV USG 2.5/5/12V Process			

Chapter 4

Design of High Voltage Generator

4.1 Introduction

As mentioned above, not only current mode but also voltage mode need the need a high supply voltage to perform stimulation. So the stimulator system also contains a fully on chip high voltage generator, and the high voltage generator is integrated with stimulator on the same chip too. The high voltage generator in stimulator system is show in Fig. 4.1.1.

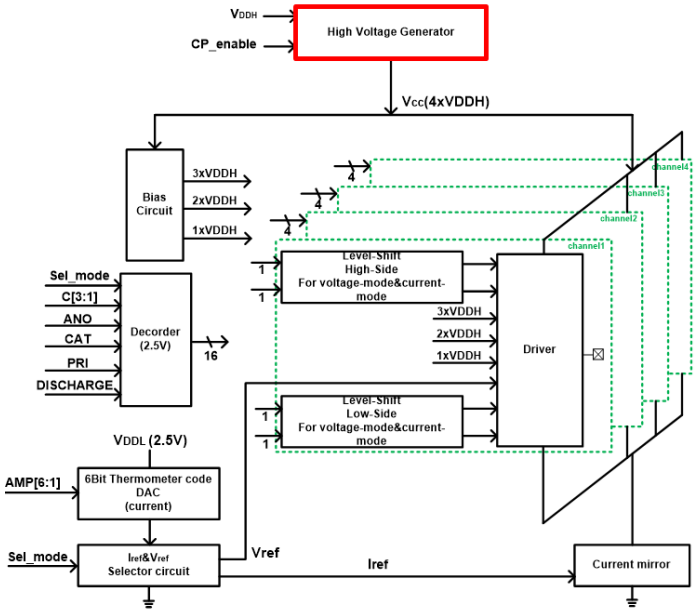


Fig. 4.1.1 The high voltage generator in stimulator system.

4.2 Prior Arts of Positive Charge Pump

4.2.1 Dickson Charge Pump

Fig. 4.2.1 shows the Dickson structure charge pump [30]. Dickson structure charge pump consists of diodes and pumping capacitor (C). C_P is parasitic capacitor at each node and C_{out} is output capacitor. When clk is high (means clkb is low), the even stage diodes are turn on, the odd stage diodes are turn off. Similarly, when clk is low (means clkb is low), the even stage diodes are turn off, the odd stage diodes are turn on. Through this mechanism, the charge can be delivered from front stage to the next stage alternately. Due to the parasitic capacitor (C_P), the voltage swing of each node is the clock swing (V_{clk}) divided by the ratio of C and C_P. The voltage drop of each stage can be expressed as (4.1). V_D is the diode forward voltage drop, so the voltage fluctuation of each stage can be shown as (4.2). If for N stage Dickson charge pump situation, the output voltage is shown as (4.3).

$$\Delta V_{drop} = \frac{I_{load}}{f(C+C_P)} \tag{4.1}$$

$$\Delta V = V_{clk} \times \frac{C}{C+C_P} - \frac{I_{load}}{f(C+C_P)} - V_D \tag{4.2}$$

$$V_{out} = N\left(V_{clk} \times \frac{C}{C+C_P} - \frac{I_{load}}{f(C+C_P)} - V_D\right) - V_D \tag{4.3}$$

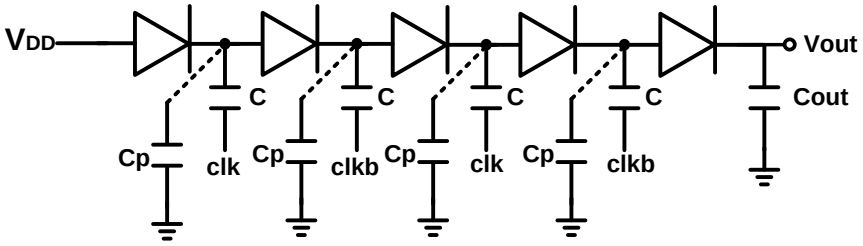


Fig. 4.2.1 Dickson charge pump with diode.

Fig. 4.2.2 is the Dickson structure charge pump with NMOS [31]. Dickson structure NMOS charge pump consists of diode connected NMOS and pumping capacitor (C). Similarly, C_P is parasitic capacitor at each node and C_{out} is output capacitor. But the different point of diode one, the voltage drop of each stage is MOS threshold voltage (V_t), this value usually smaller than diode voltage drop V_D. So, the efficiency of this NMOS structure is more high than diode one. Moreover, if the NMOS body don't connect with MOS source, it has body effect, which may increase threshold voltage (V_t) and decrease the efficiency. The maximum voltage difference between MOS source and drain is $2V_{clk}$-V_t. In low voltage process, the MOS will suffer from gate-reliability issues.

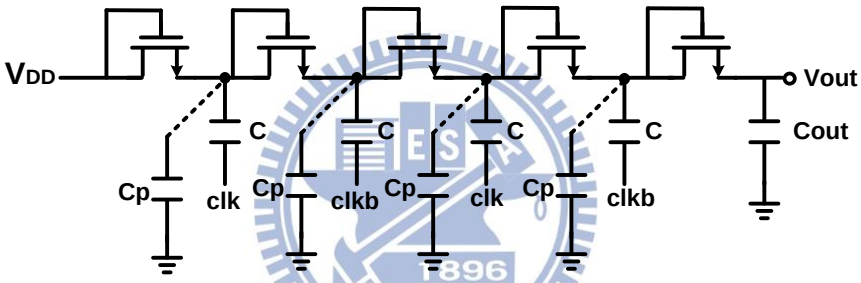


Fig. 4.2.2 Dickson charge pump with NMOS.

4.2.2 Cross-Couple Charge Pump

In order to overcome gate-oxide reliability issues, overcome threshold voltage drop and to improve pumping gain and efficiency, some charge pump circuits were proposed. Fig 4.2.3 shows the cross-couple charge pump [32], which was designed without overstress voltage across MOS and realized in low voltage CMOS process.

When clk is low (means clkb is high), the voltage of node 1 become V_{DD} and the voltage of node 5 become $2V_{DD}$ due to clkb. At the same time, Mn1 is turned on and Mp1 is turned off. Mn5 is turned off and Mp5 is turned on. The voltage of MP1's drain become $2V_{DD}$.

By the operations, the voltage can be pumped high without gate-oxide reliability issues. Moreover, this circuit doesn't have threshold voltage drop by using MOS switches to transfer charge. Besides, this circuit used two branches (means equivalent working frequency is double), which can have less output voltage ripple at the output.

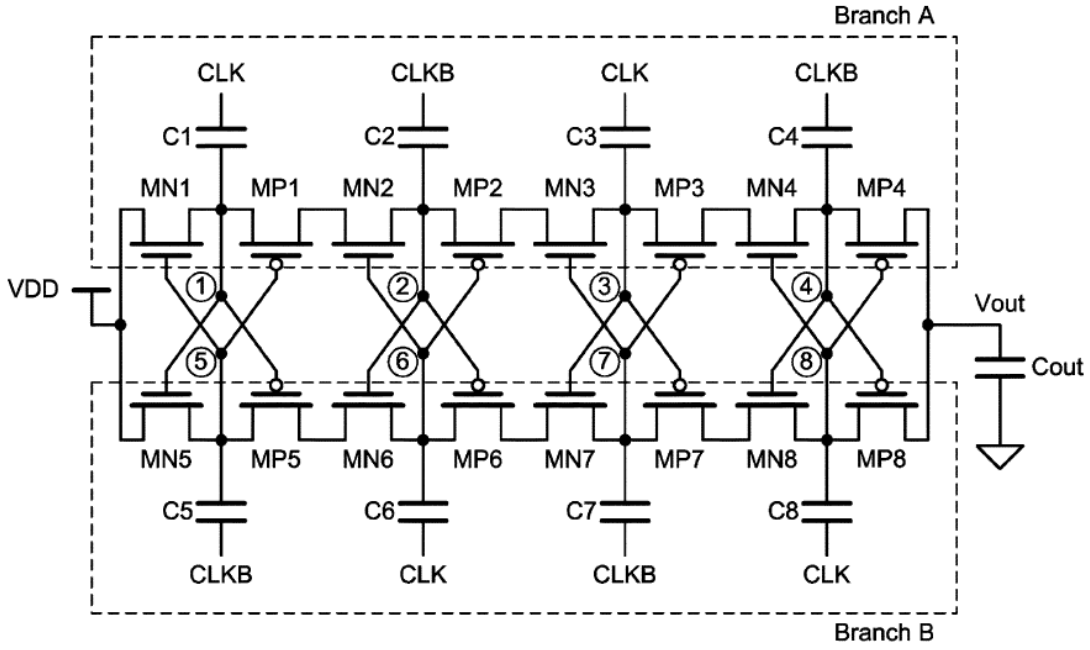


Fig. 4.2.3 Cross couple charge pump.

4.3 Design of Positive Charge Pump

4.3.1 The PFM Charge Pump System

The PFM charge pump system is show in Fig. 4.3.1, by using feedback control to maintain the expected output voltage. For example, when output load becomes heavier, the output voltage will decline. But it promote the analog input voltage of the VCO, the pumping clock become faster, it will cause output voltage increase. So the output voltage can maintain in a range by using feedback control. Moreover, when output load heavier, the working frequency is higher too (A typical PFM system).

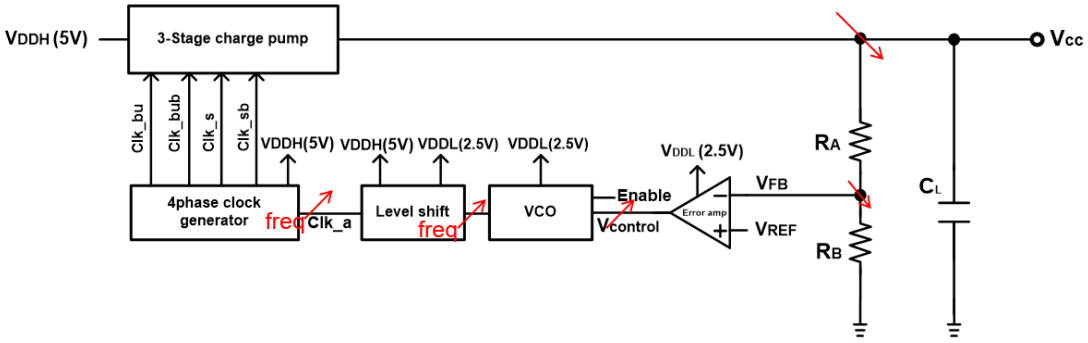


Fig. 4.3.1 The PFM charge pump system block diagram.

4.3.2 The main 3-Stage Charge Pump

The main architecture of charge pump can improve the reverse current problem in four-phase cross-couple charge pump [33]. But it needs four non-overlap clock to achieve the function of reduction of reverse current. The relative order of four clock and the 3-stage charge pump circuit are show in Fig. 4.3.2.

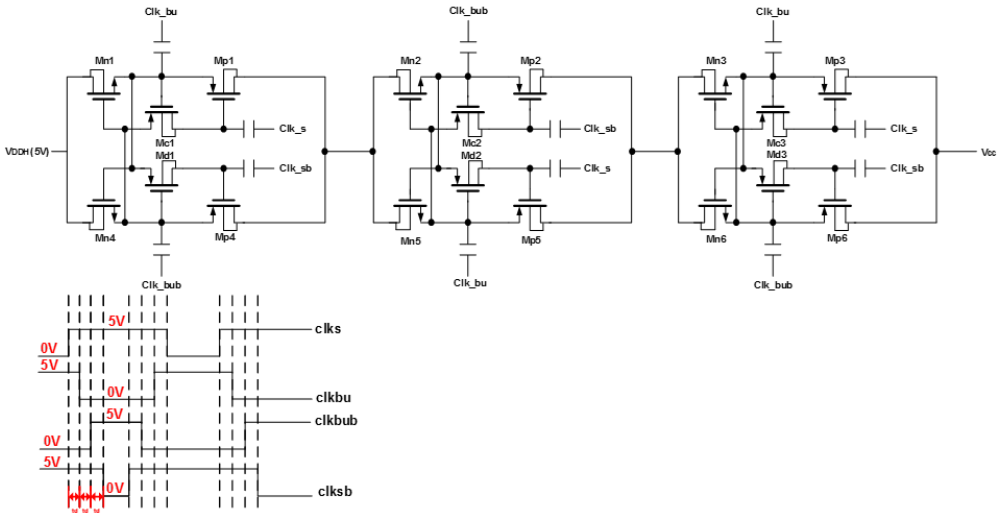


Fig. 4.3.2 The main 3-stgae charge pump.

4.3.3 The Error Amplifier

For the speed consideration of loop, the error amp is one stage structure. Just like two stage CMOS op-amp, the two stage CMOS op-amp includes constant gm circuit to generate current source and start-up circuit to avoid problem of zero current. Because the structure is one stage, there will be one pole appears in the two stage CMOS op-amp. Thus frequency compensation is not needed, and its unity gain frequency must higher than two stage op-amp. So it can meet the speed consideration of loop.

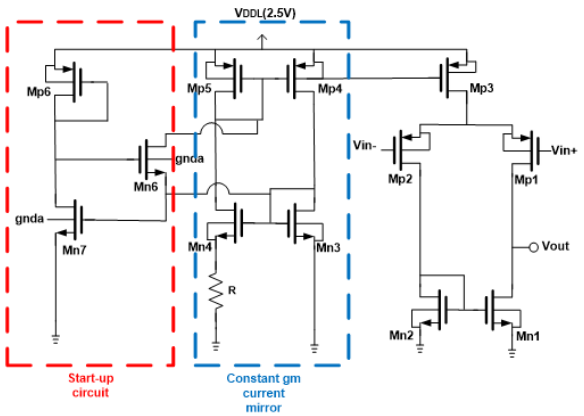


Fig. 4.3.3 The error amp in PFM charge pump system.

4.3.4 The Four Phase Clock Generator

Fig. 4.3.4 show the four phase clock generator. For non-overlapping, the specific delay cell like 2*delay and 1*delay is put into suitable location, so it can make three equal delay time.

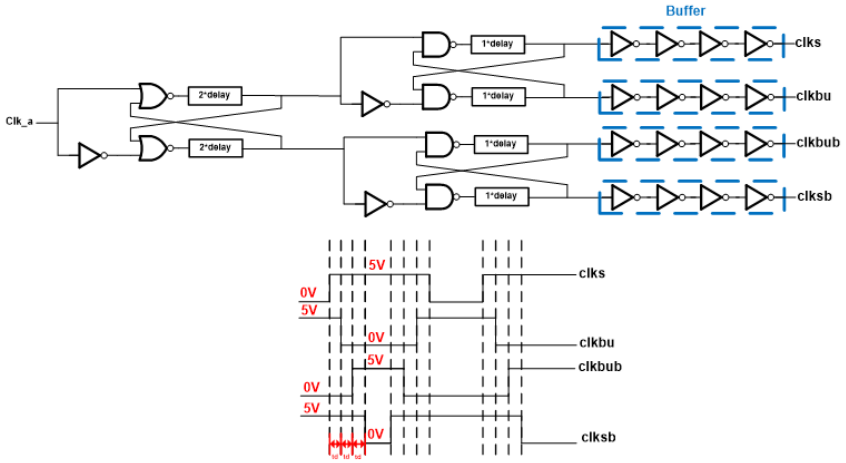


Fig. 4.3.4 The 4-phase clock generator in PFM charge pump system.

4.4 Simulation Result

Fig. 4.4.1 show the simulation result under output load is 0.5mA. The close loop working clock frequency is about 4.4MHz, and the output ripple is 256mV. The output voltage is 18.049V and the efficiency of this case is 69.429%.

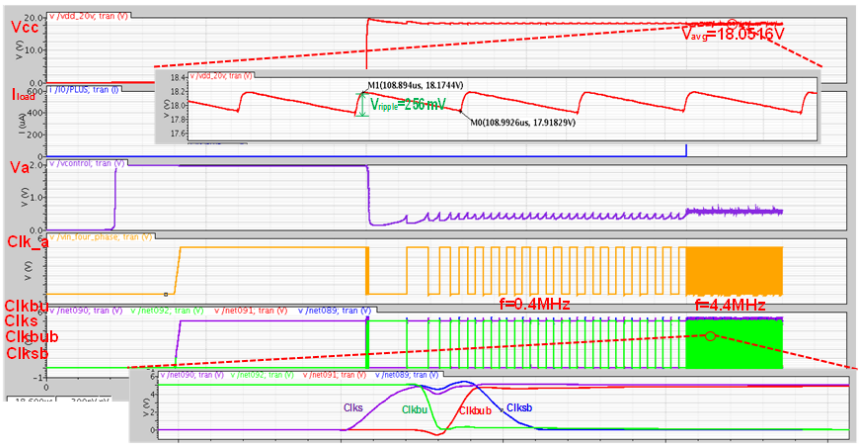


Fig. 4.4.1 PFM charge pump simulation result under output load=0.5mA.

Fig. 4.4.2 show the simulation result under output load is 5.5mA. The close loop working clock frequency is about 55.3MHz, and the output ripple is 130mV. The output voltage is 18.026V and the efficiency of this case is 69.426%.

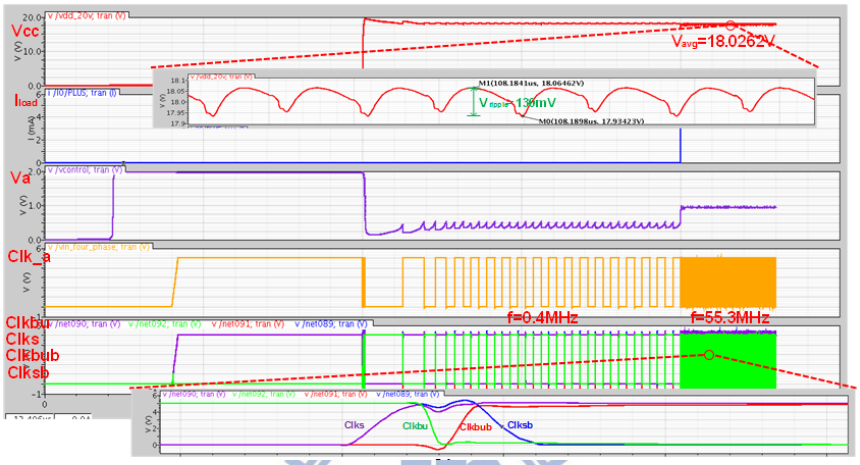


Fig. 4.4.2 PFM charge pump simulation result under output load=5.5mA.

4.5 Measurement Result

Fig. 4.5.1 shows the measurement setup of PFM charge pump. Agilent B2902A (power supply) is used to provide the fixed voltage 2.5V (V_{DDL}) and 5.0V (V_{DDH}) and observe the input current to calculate the efficiency of charge pump. Tektronix MSO 5104 (oscilloscope) is used to observe the output voltage waveform of the charge pump.

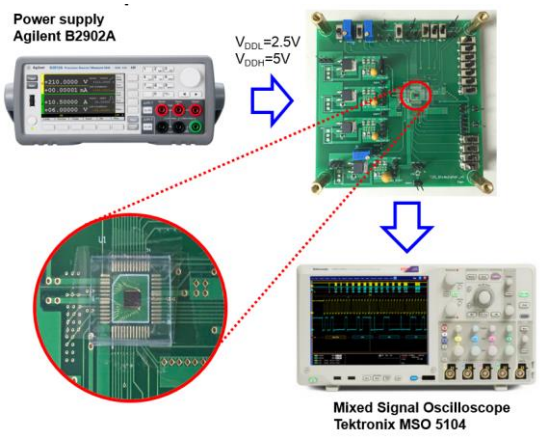


Fig. 4.5.1 The measurement setup of PFM charge pump.

Fig. 4.5.2, Fig. 4.5.3 and Fig. 4.5.4 show the different case of output load. These load current are 1mA,3mA and 5mA respectively. Obviously, the average output voltage, output ripple decrease and working frequency increases when output load increase, this is standard PFM power system feature.

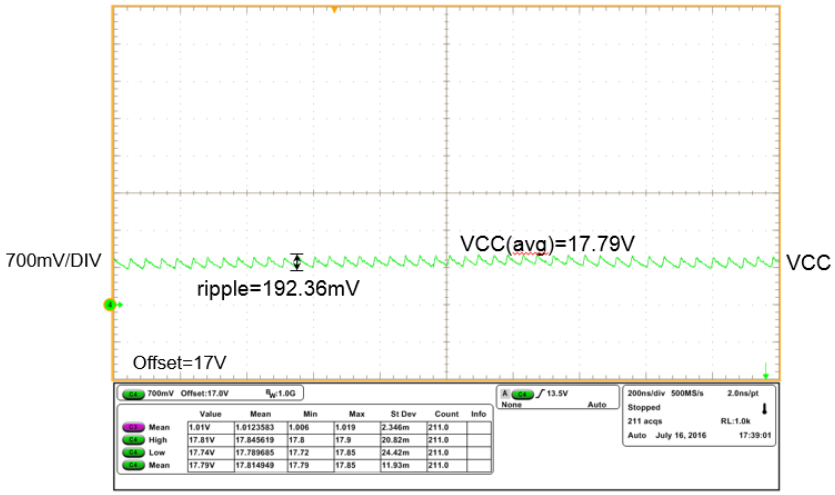


Fig. 4.5.2 PFM charge pump measurement result under output load=1.0mA.

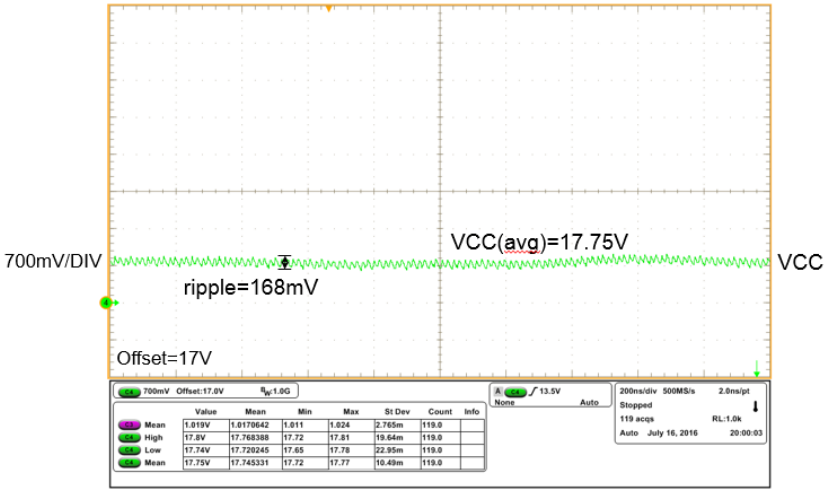


Fig. 4.5.3 PFM charge pump measurement result under output load=3.0mA.

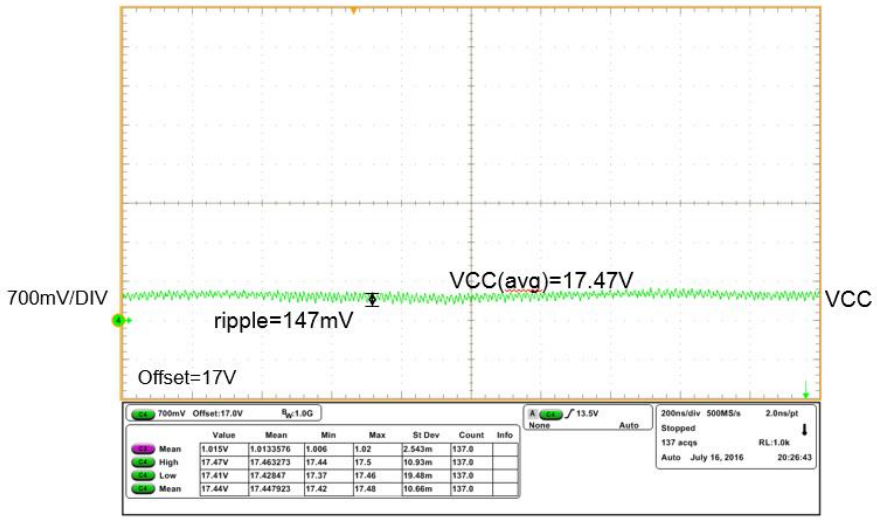


Fig. 4.5.4 PFM charge pump measurement result under output load=5.0mA

4.6 Summary of Positive Charge Pump

Table 4.1 summarizes the PFM positive charge pump specifications. Although the efficiency of measurement is lower than pre-layout simulation about 5%, the efficiency of all loading case still can exceed 60% and output voltage can achieve about 17.5V.

Table 4.1

Summary of PFM positive charge pump

		Pre-layout simulation (TT)	Post-layout simulation (TT)	Measurement
Power supply V_{DDL} / V_{DDH}		2.5V / 5V	2.5V / 5V	2.5V / 5V
V_{CC} / Efficiency	0.5mA	18.049V / 69.429%	18.044V / 66.302%	17.891V / 63.328%
	1.0mA	18.045V / 70.420%	18.041V / 66.720%	17.798V / 64.152%
	2.0mA	18.038V / 71.431%	18.036V / 67.055%	17.765V / 64.832%
	3.0mA	18.034V / 71.685%	18.031V / 67.432%	17.753V / 65.326%
	4.0mA	18.032V / 71.383%	18.028V / 67.058%	17.688V / 64.560%
	5.0mA	18.028V / 70.312%	18.023V / 66.556%	17.553V / 63.328%
	5.5mA	18.026V / 69.426%	18.019V / 66.358%	17.479V / 62.823%
Process			0.25-μm HV USG 2.5/5/12V Process	

Chapter 5

Conclusions and Future Works

5.1 Conclusions

This chip realized dual-mode stimulation, it can generate 0.1mA~5mA(per 0.1mA step) in current mode and 0.5V~10V(per 0.5V step) in voltage mode, and two modes can operate on the same chip through mode select pin.

For different pathological needs such as: epilepsy suppression, cochlear implants, Parkinson's disease, using of different stimulation method can achieve different treatment effects, and investigate each symptom preferred stimulus patterns and methods. Moreover, to wafer these functional electrical stimulation instrument currently on the market which also have a dual-mode function will bring advantage of volume and cost. Besides, for different pathological needs such as: epilepsy suppression, cochlear implants, Parkinson's disease, using of different stimulation method can achieve different treatment effects, and investigate each symptom preferred stimulus patterns and methods.

Overstress problem is also taken into account. As mentioned above, all the device do not suffer from overstress problem when operating in current mode or voltage mode.

The high voltage of stimulator system (about 17V~18V) is also generated by PFM charge pump system. And the PFM charge pump efficiency is about 60% under output load range form 0.5mA~5.5mA. Moreover, the PFM charge pump is fully on-chip.

5.2 Future Works

5.2.1 Impedance Detection System

The impedance detection system can detect the equivalent electrode model just like the value of R_s and C_{dl} through ADC circuit. Getting the information of impedance value and also know the current amplitude of stimulation, it can be calculated the enough value of Vcc through decoder. Then decoder can control the positive or negative charge pump stage to generate the desired V_{CC} or V_{SS}, in other words, pumping to highest voltage is not always necessary. This feature can greatly enhance the efficiency of whole stimulator system. Moreover, by using the impedance detection system, if the abnormal value of impedance such as (open or short) is detected, the disable signal can control stimulus driver to stop the stimulation and prevent the tissue damage. The brief illustration block diagram is show in Fig. 5.2.1.

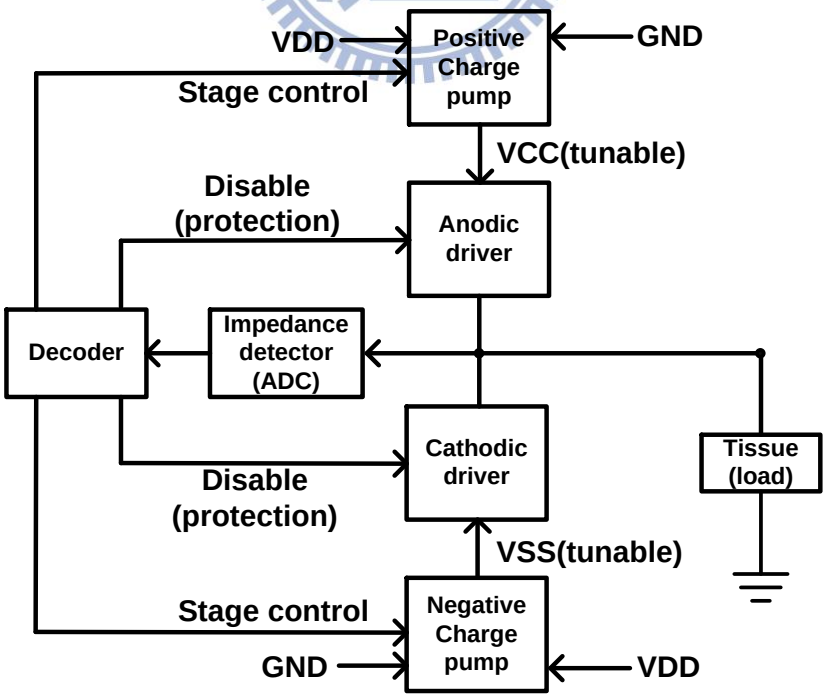


Fig. 5.2.1 Architecture of impedance detection system.

5.2.1 Parkinson's Disease Application

For Parkinson's disease application, the voltage stimulation waveform is needed [10]. By using FPGA or MCU to make specific D[6:1], ANO and CATH signals. Then controlling the stimulator chip to generate ramp of voltage stimulation waveform. On the top of Fig. 5.2.2 shows the brief architecture of whole system. The middle of Fig. 5.2.2 shows the brief output voltage waveform. When enable signal is rising edge, the stimulation waveform should ramp up. If the enable signal logic high time is long enough, the stimulation waveform should hold after ramp up. If the enable logic high time is not long enough, the stimulation waveform should ramp down immediately when enable signal is falling edge and will not go into holding stage. Bottom of the Fig. 5.2.2 shows detail of output waveform, every tone is the biphasic stimulation pulse. And pattern of pulse is decided by the rising, falling edge and the logic high time of enable signal.

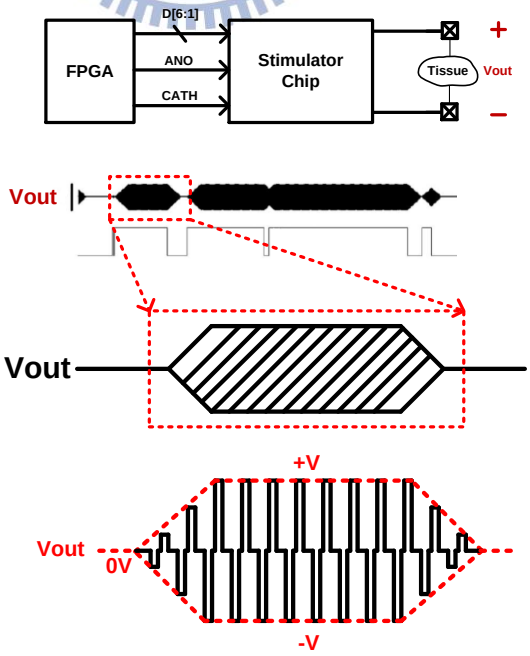


Fig. 5.2.2 Voltage stimulation pattern for Parkinson's disease application.

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