國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩士論文

高壓製程之靜電放電防護元件設計

Study of Electrostatistic Discharge Protection Devices in High-Voltage BCD Processes

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中華民國一〇三年三月

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碩士論文

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摘要

高壓元件已在各種產品(電腦、消費性、通訊、和車用電子產品)中被廣泛的運用，LED、車用安全控制晶片、電源管理晶片、觸碰螢幕控制晶片和太陽能元件都是很好的例子，將來這樣的應用將會與 IC 產業的緊密結合。隨著高壓元件市場需求量日與劇增，連帶的對於高壓元件的靜電放電防護可靠度設計的需求也非常高。在積體電路製造、封裝及測時的時候，都有可能受到靜電的轟擊，隨著元件尺寸縮小，這樣的危害更為明顯。現今，靜電放電所造成的可靠度議題漸漸的被重視。為了避免靜電來襲將會導致元件不正常工作甚至損壞，添加或更改元件結構使其滿足靜電防護的標準將是一個十分重要的課題。

在高壓製程中靜電防護的研究尤為困難。因為高壓的靜電放電防護元件需同時滿足耐高壓及大電流的能力，又要防止閂鎖效應 (latch up)的發生。橫向擴散電晶體(LDMOS) 常在高壓互補式金氧半製程中被使用，倘若其能同時工作和當作靜電防護元件將會省去許多面積。然而，在高壓製程中有諸多變因會導致靜電防護能力的下降，例如克爾克效應 (Kirk-effect)導致保持電壓(holding voltage)太低、元件的不均勻導通：導致電流過於集中某處所造成永久性的損害、氧化層的載子侷限效應(oxide charge trapping)等等造成其高壓元件本身難有良好之靜電放電防護能力，在這個因素之下，即使將靜電放護元件布局面積放大，

也不一定會獲得耐受度的提升。不均勻導通的原因，有可能是因為其保持電壓太低的緣故，提升元件的保持電壓，既可能可以改善不均勻導通的現象，也能夠防止雜訊導致的閂鎖效應，但由於熱的效應，提升電壓很容易導致可排放之靜電放電電流下降。因此如何在不減損原本靜電防護能力的前提之下提高其保持電壓，也是高壓靜電防護元件設計的一大課題。

如何設計最佳化的高壓靜電放電防護元件，是本論文的探討重點。在這次碩士論文，提出了許多不同結構形式的橫向擴散電晶體(LDMOS)，希冀能透過研究，找出橫向擴散電晶體的最佳結構能夠滿足同時正常工作和自我保護的要求。其透過第三章的研究結果可以發現，在汲極端加以改良設計過後的元件能成功的使寄生的矽控整流器(SCR)成功的出現，也因此該元件的靜電耐受度能夠過人體放電測試 2kV 的靜電防護標準。另外，先前提到的不均勻導通及閂鎖效應均歸因於保持電壓太低，這個問題尤以含有寄生矽控整流器的元件中最為明顯。因此有許多提升保持電壓的方法將在本論文的第四章中被提出，透過實際下線量測的結果可以發現，在源極中多加上一個寄生雙極性電晶體的結構能夠使保持電壓有效的提升，搭配其他參數的變化，就能夠發展出許多不同的靜電防護元件。本碩士論文所提出結構也已經有相對應的國際期刊與會議論文發表。

Study of Electrostatistic Discharge Protection Device in High-Voltage BCD Processes

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Abstract

Nowadays, with a rapid increase in demand, such as motor drivers, LED lighting, solar energy and display driver circuits, high voltage integrated process technologies have been developed and become commercially available. The lateral DMOS (LDMOS) is a common device for high-voltage output driver. Thus, LDMOS was expected for self-protection electrostatic discharge (ESD) device. ESD is an inevitable event during fabrication, packaging and testing processes of integrated circuits. ESD protection design is therefore necessary to protect ICs from being damaged by ESD stress.

In the last two decades, some studies shows that ESD robustness of nLDMOS is not good in the results of Kirk-effect-induced holding voltage lowering, multi-finger non-uniformity issue and isolation oxide charge trapping issue. Though the ESD performance is not good enough, gate-grounded-LDMOS in ESD condition is widely used due to straightforward implementation and sufficient high current

capabilities. Developing a HV-LDMOS that can meet the acceptable ESD level without scarifying the IV characteristics and dimension of the device will be a big challenge for smart power technologies.

In this work, many different structures of nLDMOS have been realized in 0.25-μm 60-V BCD process including source-side and drain-side engineering. Also stretch the layout parameter and style to optimize the nLDMOS's ESD robustness. The structure that combines the concepts of changing the layout space and embedded SCR inside LDMOS with additional p+ and n+ implantation regions between its drain and poly-gate to make sure that it can keep stably in the high-current holding region and meet the typical ESD specification of commercial IC products.

Owing to the superior ESD performance of SCR, the device structure in Chapter 4 is based on embedded SCR structure in both HV and LV well. Hoping to figure out a device that can have good ESD levels and latchup immunity, this work investigates the different structures and parameters of HVSCR and LVSCR by many different methods to increase the holding. All the devices are successfully verified in a 0.25-μm 60-V BCD process.

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黃楀晴

謹誌於竹塹交大

民國一零二年六月

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Chapter 1

Introduction

1.1 Motivation

High-voltage operations are often used in the industrial applications, such as automotive electronics, green energy, power management ICs, and industrial control. Electrostatic discharge (ESD) protection in smart power technology is a very challenging task due to its high operation voltage and an insufficient ESD design window as shown limited by both operation voltage and the failure voltage of the component to be protected [1]. That means the ideal ESD power clamp should have low trigger-on-voltage,high immunity for latchup and enough margin for reliability under high voltage operation. Typical specification for integrated circuits requires at least 1kV HBM on all pins, according to the recent recommendation of the Industry Council on ESD target levels in HV device while many customers are still requesting the former 2kV HBM level [2].

One of the most popular structures in high-voltage process is the Lateral Diffused MOS (LDMOS) which is widely used as an output driver. LDMOS was expected to have self-protected capability against ESD. However, owing to the high process complexity and fabrication cost in HV process, it is difficult to guarantee the ESD reliability of HV devices. Tough LDMOS doesn't have good ESD robustness initially;the gate-gounded-NMOS is still widely used as ESD protection device due to straightforward implementation and sufficient high current capability. Therefore, developingnLDMOS or other ESD protection devices that can meet the acceptable ESD level without scarifying the IV characteristics and dimension of the device will be a big challenge for smart power technologies.

1.2 Introduction of Electrostatic Discharge (ESD)

ESD is critical stress event for semiconductor products, which can encounter during manufacturing, packaging or assembling process [3]. It is an instantaneous discharging of electrostatic charges on IC pins by physical touching of a human body, contacting of manufacturing machines, or discharging of on IC chips itself. According to the different discharge conditions and sources of electrostatic charges, ESD can be classified to human-body model (HBM), machine-model (MM), and charged-device model (CDM).

(1)Human Body Model (HBM)

HBM is a common ESD event due to the connection of a charged human body and an IC product. If the electrostatic charge transfers into the IC products, the device may get some damage. To prevent the failure, the human body model is established to simulate this kind of stress by the equivalent schematic in Fig. 1.1 [4]. In the equivalent circuit for HBM ESD event, a 1.5 kΩ resistor and the 100-pF capacitor are placed to represent the parasitic resistor and capacitor of a human body. Commercial ICs are generally demanded to pass 2-kV HBM level.

(2) Machine Model (MM)

The MM ESD event arises from the contact of a machine and IC products. The equivalent circuit diagram of MM ESD event is shown in Fig. 1.2 [5], where there is no equivalent resistor on the equivalent discharging path. Commercial ICs are generally demanded to pass 200-V MM level.

(3) Charged Device Model (CDM)

The CDM ESD event happens under the condition of the contact of charged IC and external grounded object. During the process, some charge would store in the p-substrate. When this charged IC is touched by an external grounded object, CDM charges in the p-substrate will be discharged from the IC inside to the

grounded object outside. There is no standard equivalent parasitic capacitor and resistor for the CDM ESD stress because different dimension of chips, different form and size of packages result in different values of the parasitic capacitor and resistor of IC chips. A commercial IC is generally requested to pass at least 1-kV CDM ESD stress, which can generate an ESD current with peak current value about 15 A within a rise time less than 200 ps[6].

(4) Transmission Line Pulse (TLP) System

The TLP system applies the voltage pulse to the device under test (DUT). The oscilloscope measures the voltage and current during the TLP stress, and then the source-meter measures the leakage under certain bias condition. The steps above are sequentially repeated with increasing TLP pulse amplitude until the device satisfies the failed criteria.

TLP is common system in ESD protection studybecause the system providesmore details about the I-V characteristic of the device. I-V curve measured by TLP systems can give an ESD protection design window to let IC designers choose the right device easily. ESD protection design window of ESD protection device is shown in Fig. 1.3 [7]. Trigger point represents the triggering of parasitical bipolar junction transistor (BJT), which is needed below the gate oxide breakdown voltage to ensure successfully protection. After trigger, the device gets into the snapback region. The lowest voltage after the parasitic device triggering on is called holding voltage. The holding voltage should higher than the normal operation voltage to accomplish a latchup free design [7]. Secondary breakdown current (It_2) is the maximum current handling ability of the device. In other words, the device willbe fail as after It_2 point. The TLP result of It_2level is proportional to HBM level.

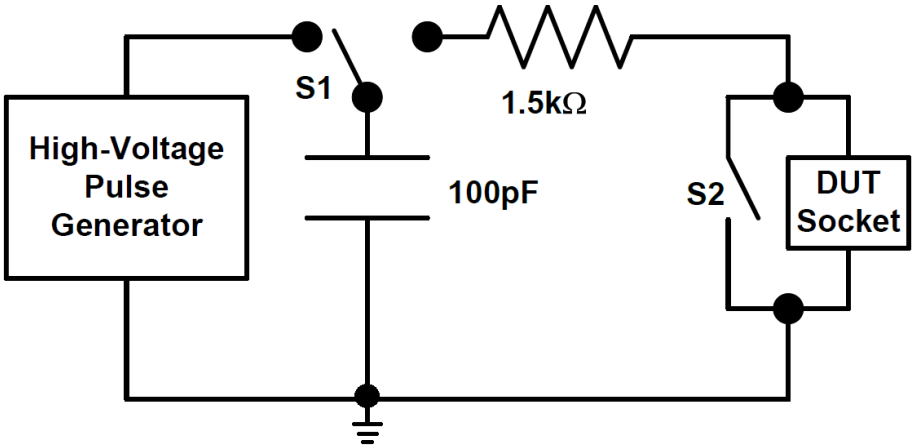

Fig. 1.1 The equivalent circuit of the human body model ESD event [4].

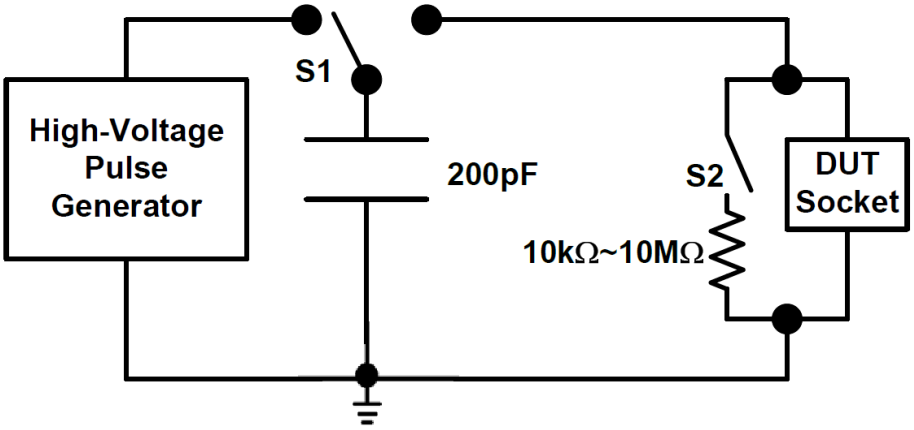

Fig. 1.2 The equivalent circuit of the machine model ESD event [5].

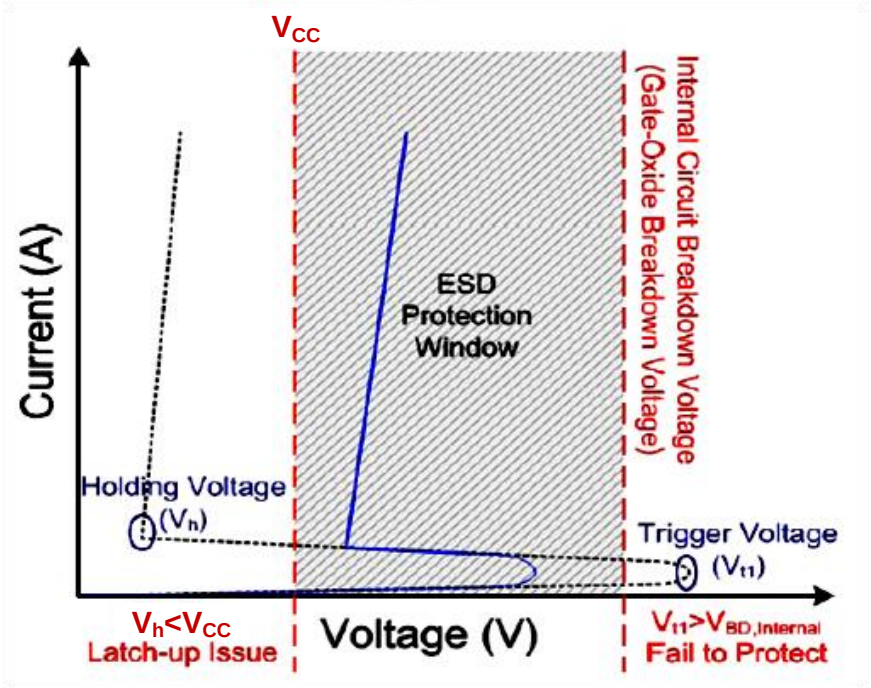

Fig. 1.3 ESD protection design window ofESD protection device [7].

1.3 Thesis Organization

Chapter 1introduces the motivation of this work,basic background knowledge of ESD protection design and the thesis organization.

Chapter 2 shows some common ESD protection devices and their characteristics in HV process. Furthermore, some restrictions and limitations of those devices and their applications have been reported. Then introduce some background knowledge of SOA which is one of the hot topics in high voltage process. Also report the trade-off between ESD and SOA. Those issues confine the ESD performance in high voltage applications. The following chapters try to find out the optimized solutions in high voltage ESD protection.

In Chapter 3, thereare many different structuresof nLDMOShave been realizedin0.25-μm 60-V BCD process. Those devices' ESD robustness will be discussed. Furthermore, failure analysis has been down for some specific device structures.

In Chapter 4, investigating how the different layer and parameter affect the HVSCR and LVSCR. To prevent thelatchup issue, many different method of increasing holding voltage have been discussed. All the devices aresuccessfully verified in a 0.25-μm 60-V BCD process.

Finally, the conclusions and some suggestions for future investigation have been indicated in Chapter 5.

Chapter 2

Overview for High voltage ESD protections

2.1Common ESD Protection Device in High Voltage Process

To protect integrated circuit to against ESD, IC designers would use several ESD protection devices in HV process. Some of them can protect themselves, which means it can both operate in normal condition and protect itself when ESD happens. Some of them are placed just to protect the integrate circuit without any function. The self-protection device is more straightforward. Some structure may not capable of being self–protected for ESD specification.Then additional ESD protection circuit is one of the possible solutions. In that case, the trigger voltage of ESD protection device should be higher than VDD. On the other hand, the protection mechanism must turn on below the breakdown voltage of the internal circuit or the gate-oxide breakdown voltage. The competition between the ESD protection circuit and output array usually have bad ESD result. Plus the area concern, self-protected device are preferable to HV technologies. This limitation also indicates that the holding voltage should be higher than the operation voltage and therefore cause high power dissipation and lower ESD failure currents[8].

Those ESD protection devices can be categorized into five main types below.

(1) Diode

Diode has been used as an ESD protection device for a long time. I-V characteristic of diode behavior during the ESD condition is depicted in Fig. 2.1(A). In the reverse bias region, once the voltage across the device is large enough to breakdown the junction, there forms the path to discharge thecurrent.

This kind of ESD protection devices would not snapback, which means the holding voltage is higher than the breakdown voltage.The success or failure of the affair is all due to the high holding voltage.Higher holding voltage ensures the latchup immunity but let the device has lower ESD robustness. The thermal capacity of the device per micron is fixed. So the higher holding voltage leads to the lower current level. Since the ESD robustness of diode per micron is rather low,enlarge the size of diodeis one of the solutionsto pass ESD criterion. But drawingthe diode device in a large size not only wastes the chip area but also causes a higher capacitance and leakage currents in normal condition.

(2) P-type MOS or FOD

The behavior of P-type devices during the ESD condition is similar to the reverse diode. I-V curve is shown in Fig. 2.1(B). The ESD robustness is very process dependent. In some process, P-type device has the higher ESD levels per micron than the diode. As a result, using the P-type device as an ESD protection can have both relative lower silicon area consumption and leakage with latchup immunity.

Because of the limitation of ESD design window, the non-snapback device such as PMOS and PNP FOD are usually used in high voltage process to fit those constrains of ESD protection window. In this kind of devices, the uniform turn on in such the large size is the main issue.

(3) nLDMOS or **N-type** FOD:

The N-type lateral DMOS (nLDMOS) is a common device for high-voltage output driver. nLDMOS can also be the protection device during the ESD due to its parasitic bipolar junction. When the voltage across the MOS is higher than the breakdown voltage of the reverse drain/body junction, drain leakage current

starts to increase apparently due to the avalanche generation. The voltage corresponds to 1-uA leakage current is defined as the breakdown voltage. After breakdown, the LDMOS acts like a diode in reverse bias region. The peak of electrical field lies on the interface between HVPW and HVNW. The voltage across the MOS keeps increase until the avalanche generation current through the junction of body and source is large enough to forward bias the parasitic diode between body and source.Once the parasitic NPN junction turns on, the voltage across the device is clamp down to the holding voltage. This is called device snapback. I-V characteristic behavior of nLDMOSin ESD condition is depicted in Fig. 2.1(C).

In the last two decades, some studies show that nLDMOS ESD robustness is not good enough in the results of some issues such as Kirk-effect-induced holding voltage lowering, multi-finger non-uniformity issue, or low breakdown voltage due to isolation oxide charge trapping [9], especiallyin some applications. Plus, the large difference between the trigger voltage and holding voltage leads to multi-finger non-uniformity issue. As one finger of the nLDMOS turns on first, this fingers would get into the snapback region immediately and pulls down the voltage. Then the electrical fields of the other fingers are too low to turn on the other npn bipolar transistors any more [10]. Commonly this is attributed to non-uniform turn-on behavior.Some techniques have been introduced to improve the ESD robustness of nLDMOS by enhance the uniformity of the multi-finger, such as high-resistance-body shallow trench isolation (STI), source ballasting, substrate/gate biasing [11], weakly snapback method, and so on [12]. The main concept of those techniques are reducing the difference between trigger voltage and holding voltage of the parasitic junction and allocating the current path more uniform. Take the field-oxide device (FOD)structure for example. Nowadays,

somesmart power technology are used N-type FODas test structures for high voltage pin applications [2], which can force the parasitic junction shows up easier.

Tough the stand-alone nLDMOSin high voltage process doesn't have good ESD robustness. Gate-gounded-NMOS is still widely used as ESD protection device due to straightforward implementation and relatively sufficient high current capability[9]. To pass the ESD criterion, it still needs some layer optimization and parameter modulation.

(4) **Device with SCR path**

I-V characteristic behavior of SCR-basedstructure is shown in Fig. 2.1(D).SCR device is known as an efficient device for electrostatic discharge (ESD) protection since it can have the highest ESD robustness in the smallest layout area. Their excellent clamping capability and high ESD robustness allow designing efficient. On the down side, most of SCR-based protections exhibit low holding voltage,which makes them prone to latchup issue. Application of the SCR device in HV technology will further deteriorate its latchup risk more seriously because of the high supply voltage operation. As a result, mistriggering of the embedded SCR imposes new reliability concerns during normal circuit operating conditions,particularly in some applications that require both high-current and high voltages at the same time [8]. The latchup event could lead to integrated circuit malfunction or even permanent destruction. The basic criterion to improve latch up immunity is to increase the holding voltage above the normal operation voltage to reach latchup-free state. The simplest improvement method is to increasethe spacing from anode to cathode, which directly increase the resistive of voltage drop across SCR [13]. Modulation of the

parasitic BJT emitter injection efficiency by reducing the emitter area is another solution. Some approachesare going to adjust the well/substrate shunt resistances [14]. Using the circuit solution, like connecting a diode string in series to raise the holding voltage, is another option.

Once the holding voltage of SCR is higher than the normal supply voltage, it will be free from latchup issue. But increasing holding voltage may decrease the ESD robustness due to the higher heat generation during ESD current discharging. Therefore, it is still a challenge to design an ESD-robust and latchup-immune SCR device within small layout area.

(5) **RC-BigFET**

If there is a big MOS in the internal circuit, using the propertyof RC delay to drives the big MOS may become an option of ESD protection. Unlike those four methods, which is mentioned above, this method turns on the MOS device itself instead of breakdown the parasitic junction to shunt the ESD current. Comparing to the operation, the ESD stress happens in a short time. Choosing the proper resistance and capacitance in the circuit can let the delay time fall within the region between the time domain of operation and ESD condition. Thus, RC delay mechanism would let the BigFET turning on to shunt the ESD current and keep off in normal condition.This dynamically triggered MOS transistormethodis commonly used in low voltage process.In high voltage process, the large area consumption of resistance and capacitance is one of concerns that make this method has relative low ESD level per micron.Also, gate coupling is another issue in high voltage applications. Using this protection method in real high voltage application still needs more devices studied and simulation.

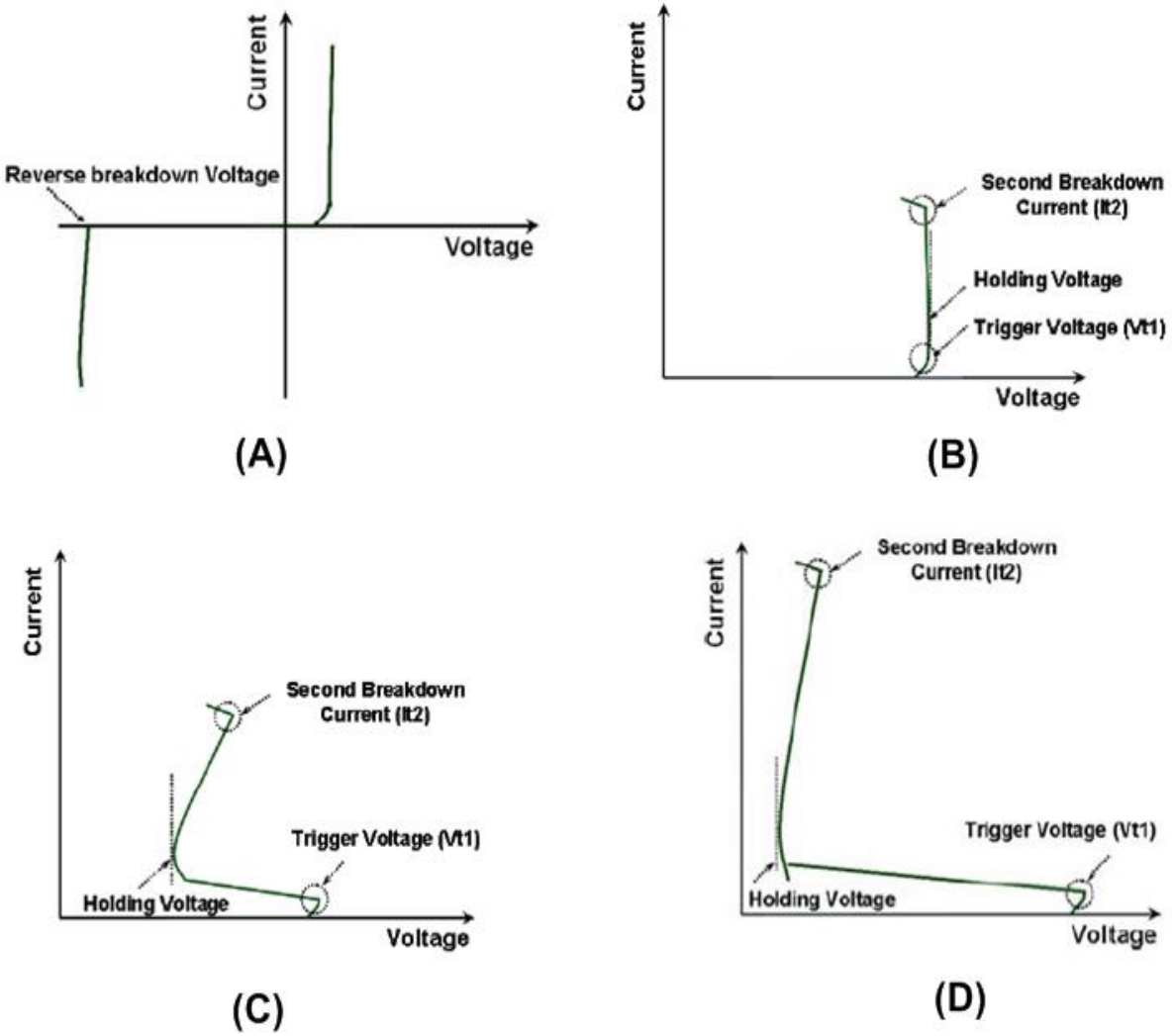

Fig. 2.1 The simplified I-V curves of the common ESD device. (A) Diode, (B) P-type MOS or FOD, (C) gate-grounded nLDMOS or N-type FOD, (D) Device with SCR path.

2.2LatchupImmunity Issue in HV Process

Ideal ESD device should have low trigger voltage, high immunity for latchup and enough margins for reliability under high voltage operation. In many HV process, the gate-grounded nMOShas much lower holding voltage than the maximum supply voltage, not to mention the embedded SCR structure. The latchup issue is one of the most critical issues in high voltage process, especially for the power camp ESD device which is placed between VCC and VSS. The worst case is that the device cannot recover without a renewed power-up cycle. In the worst case, the high DC supply current could damage the device. That is, the latchup issue prevents the application of snapback device as a power clamp device.

There are two necessary conditions for latchupoccurred. One is that the power supply current should be large enough to support the holding condition [15].Reducing the operation current can have more latchup immunity. But in some application, lower operation current would reduce the performance. The other condition to immune thelatchup issue is that holding voltageshould be higher than thesupply voltage (VCC). The difference of those two defines the latchup protection window. The basic criterion to improve latch up immunity is to increase the holding voltage. Some techniques have been proposed to increase the devices' holding voltage, such as using deep trench between drain and source or modulation of the layout spacing[1]. Once the holding is above the power supply voltage, the device would reach latchup-free state.

2.3 The Trade-off Between ESD and SOA

2.3.1 Introduction to SOA

Safe operating area (SOA) isone of the most important factors affecting device reliability[16] because the power devices may have to operate under the condition of high voltage and high current. TheSOA region defines the limitation of operating condition including voltage and current. That is, operating outside SOA region may cause some damaging of the IC products.

SOA can be roughly sorted into forward bias SOA (FBSOA) and reversed bias SOA (RBSOA). FBSOA analyzes the on-state devices and RBSOA studies the off-state devices. Unclamped inductive switching (UIS) test presents high current and high voltage across a device when it is off, so it is classified as the reverse-biased SOA (RBSOA) [17]. FBSOA is decided by the factors such as manufacture, material, package, and device structure. Electrical SOA (eSOA) and thermal SOA (tSOA) are two different mechanisms. Most of the time, electrical SOA (eSOA) boundary is important due to thermal effect is not strongly involved during operation [18].

For the device optimization, the concept of safe operation Area (SOA) under pulsed stress conditions is important. Normal operation defines the minimum form of SOA required for the qualification of LDMOS device [3].To minimize the effect of device self-heating, device under tests (DUTs) are usually stressed by the pulses with a short pulse width. A 50-Ω transmission line pulsing (TLP) system that delivers square pulses with 100-ns pulse width is usually adopted for the measurement of eSOA[8]. The setup of eSOA measurement is shown in Fig. 2.2 [19].

The SOA specification is illustrated inFig. 2.3 [19]. The SOA is formed by four curves which define respectively as follows.

(1) Line A

Line A is limited by the turn-on resistance ($R_{DS,ON}$in Fig. 2.3). Decreasing the turn-on resistance, which causes the slope increase, can have larger SOA.

(2) Line B

All devices have current carrying capability either from device itself or the wire bonding.

(3) Line C

Line C is the physical limitation. This line is determined by the current and voltage across the device with short pulse width by TLP system under fix TLP pulse width and gate bias. The equivalent circuit model of a HV NMOS is shown in Fig. 2.4 [18]. $R_{D,}$ R_S, and R_B aredrain, source, and body (parasitic) resistors, respectively. If the bias between base and emitter junction, which is generated by the current I_h, is larger enough, the BJT would be triggered on. When generated heat by P=I×V across the device excess its physical tolerance, the device would fail. Connecting the failure point with different gate bias forms the line C (like in Fig. 2.5).

Because those factors (R_D, R_S, and $R_{B)}$ have positive thermal coefficient. When pulse width increases, Line C moves downward due to the increasing device self-heating and the electrothermal coupling. Furthermore, the increasing TLP pulse width would degrade the SOA boundary.

(4) Line D

Line D is defined by the maximum voltage (BV_{DSS}) of device.

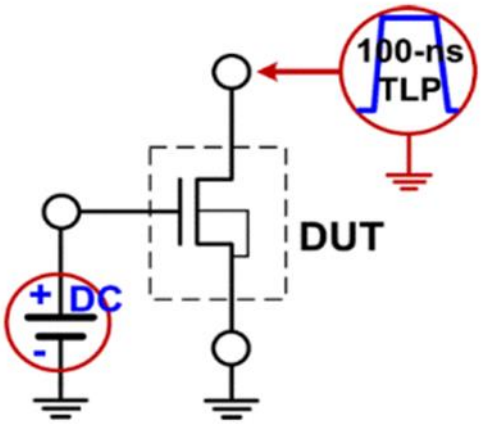

Fig. 2.2 The test setup for eSOA measurement by 100-ns TLP pulses [19].

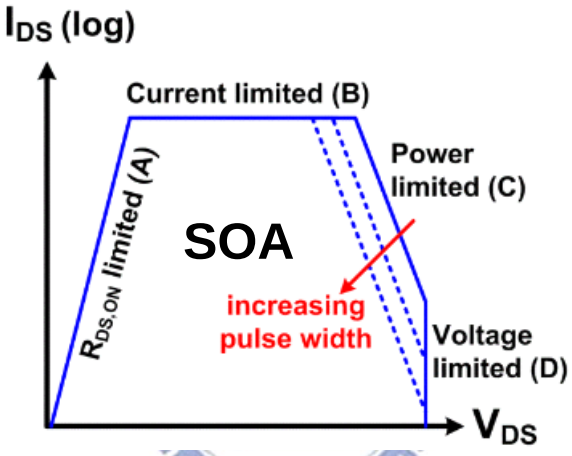

Fig. 2.3A diagram showing SOA of a high voltageMOSFET[19].

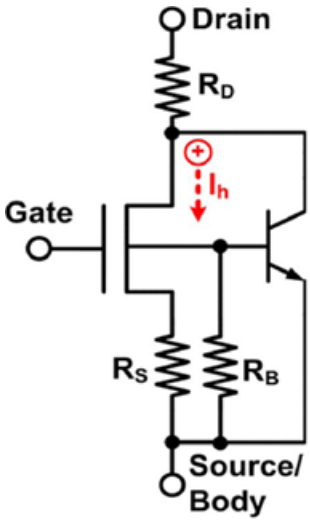

Fig. 2.4Equivalent circuit model of NMOS in high voltage process, shown with the parasitic bipolar junction [18].

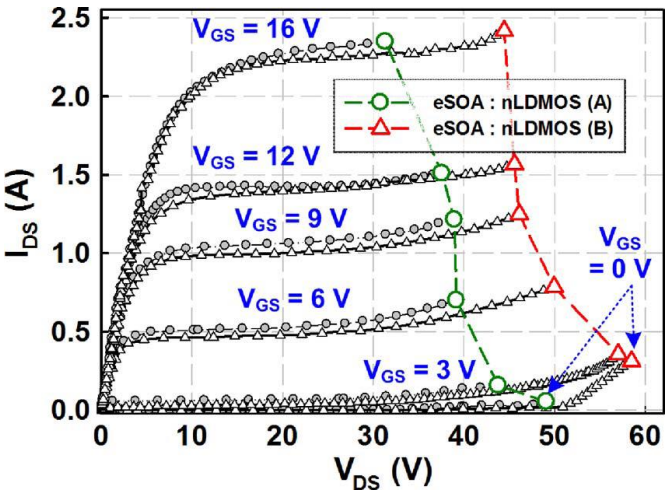

Fig. 2.5Measured SOA boundaries of two nLDMOS transistors by 100-nsTLP pulses[18].

2.3.2 Trade-off between SOA and ESD

There are three factors which can affect I-V boundary of safely switch. These factors are $BV_{DSS,}$ R_{SP} and SOA which is known as a design triangle of HV device as in Fig.2.6. Generally, the breakdown voltage and on-resistance is a well-known trade-off in HV process. Plenty of works have addressed and analyzed the tradeoff of SOA enhancement, and turn on resistance and breakdown voltage [17].

A wide SOA can enhance device reliability under load condition. Plenty of works aim in achieving the highest breakdown voltage, lowest turn on resistance, and the widest SOA for a given device size [17]. A wide SOA can sustain the high voltage and high current at the same time that happens across a power MOSFET during the circuit operations with the switching of reactive loads.Aspiring for SOA improvement becomes an increasingly important factor. Higher breakdown voltage would lead to the wider SOA. But as an ESD protection device, higher breakdown voltage may let other internal device be damaged before it shunts the ESD current. Nowadays, some process integrations use a heavily doped body region, an adaptive drift implantation, or a thick plated copper layer to improve intrinsic SOA. The previous study indicates

that additional P-type body layer, which is added to elevate the doping concentration of P-type well, can have the wider SOA when comparing to the regular nLDMOS structure.But this improving may decrease ESD robustness.For example, a heavily doped P-body region, which increases the doping concentration of P-type well in the source side, can also reduce the equivalent resistance of R_B in Fig. 2.4. Reducing R_B would result in high power dissipation and relatively weak ESD performance due to the parasitic BJT is difficult to turn on [14].That is, many high-voltage devicessuffer from early failure and limitation due to the BJT driven instability [3]. Itisimportant to have a deeper investigation on the structure of HV device to get win-win solution for SOA and ESD robustness.

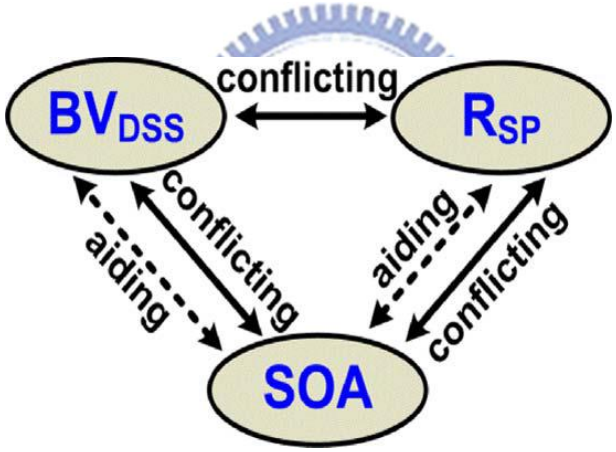

Fig. 2.6The design triangle of power semiconductor devices[18].

Chapter 3

Parameter Investigation for Self-Protected LDMOS Devices in High-Voltage Process

3.1 Standard LDMOS Structure in 60-V 0.25 μm BCD Process

High voltage and high current operations are common requirements for semiconductor devices in HV ICs.To be tolerant of high voltage across the device, there are many different light doping implantsand specific structures in different HV process. In 60-V 0.25μm BCD process, the cross-section view and top view of standardnLDMOS which foundrygives as a layout sample is shown in Fig. 3.1 and Fig. 3.2, respectively.In Fig. 3.1, the HV device is surrounded by N-buried layer (NBL) to separate HVPW and P-substrate (p-sub). So bulk ring at every source region is required to bias HVPW, the bulk side of the nLDMOS. Each 60-V nLDMOS device isolatesfrom other devices by HVNW and NBL. The channel lengths are defined by the overlapping region of p-body and the poly gate. This device is suggested to be operatein voltage region V_{DS} = 0 ~ 60V and V_{GS} = 0 ~ 5V.

One of the special implant layers of standard nLDMOS is the P-body layer. The P-body region is a highly doping layer than HVPW.The gradually doping tech(p+-p-body-HVPW) in the source side have been used to enhance the SOA region by increasing the equivalent base doping concentration of the parasitic bipolar junction transistor (BJT). Besides, the standard nLDMOSin60-V 0.25μm BCD process uses shallow trench isolation(STI) between N+ drain and poly gate instead of the traditional field oxide (FOX) to shun the bird's peak effect. This STI region can avoid the field crowding in the surface region near the drain of nLDMOS, which

increasesthe device's breakdown voltage. That is, the device can have a shorter length of the drift region is sufficient to maintain the required breakdown voltage.

nLDMOS's inherent lateral design makes it compatible with conventional CMOS process[20].Hence, it would be perfect if nLDMOS could both operate in the normal situation and protect itself during ESD. To analyze the characteristic of standard nLDMOS under HBM ESD stresses, TLP system with 100-ns pulse width is used [21].The TLP result of the standard nLDMOScell with the minimum rule is shown in Fig. 3.3.The total width of the device in this section is 800 μm.

The breakdown voltage of standard nLDMOS, which is given by foundry, is 75 V. The breakdown voltage (75 V) is around 1.2 times of supply voltage (60 V), which meets the common criteria in high voltage application. So, the standard device can be used as the operation device, but it is not robust enough to protect itself during the ESD condition. According to the TLP result, the ESD level of this device is less than 300 mA. This device would not get into snapback region until 91V. Actually, this device cannot successfully snapback before it failed.That may be the reason why the device failed in such a low ESD level.

The HBM level is around 0.5kV, which meet the experiments result of TLP test.Apparently, the ESD level of the standard nLDMOS in this 60V process is not robust enough to be the self ESD protection device. There still need more optimize design to improve the ESD performance. In the following section, this thesis indicates many different parameter modulation, source engineering and drain engineering. Optimize the nLDMOS structure to get the acceptable performance in both operation and ESD condition.

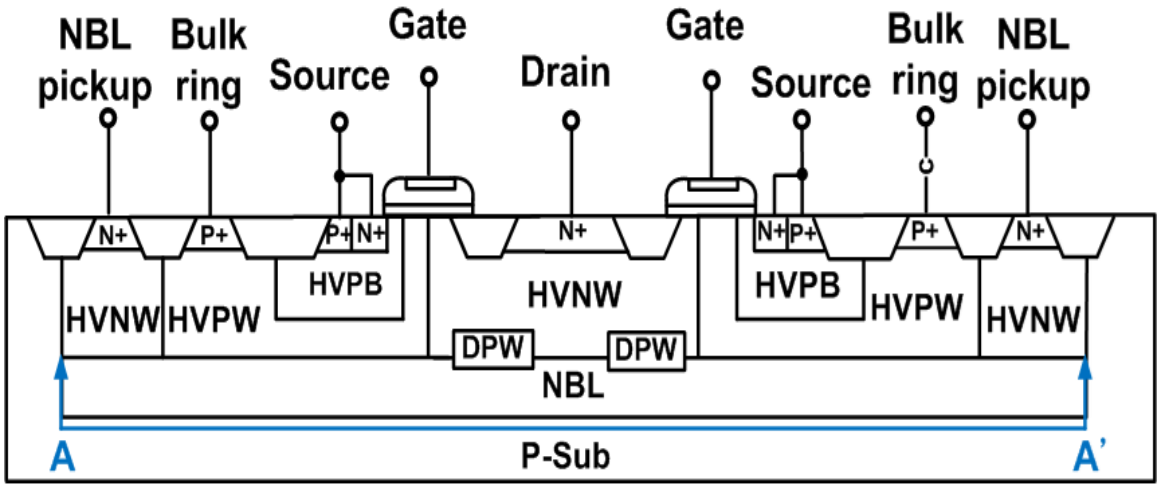

Fig. 3.1 The cross-sectionalviewof standard nLDMOS in a 60-V BCD process.

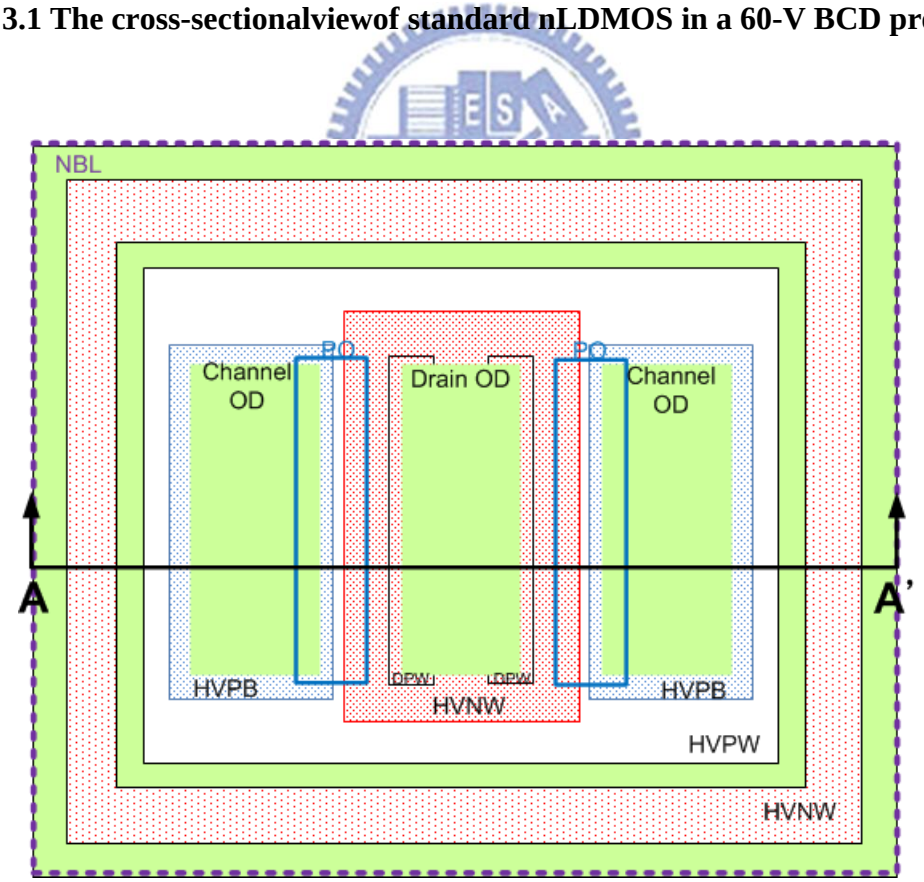

Fig. 3.2 Thetop view of standard nLDMOS in a 60-V BCD process.

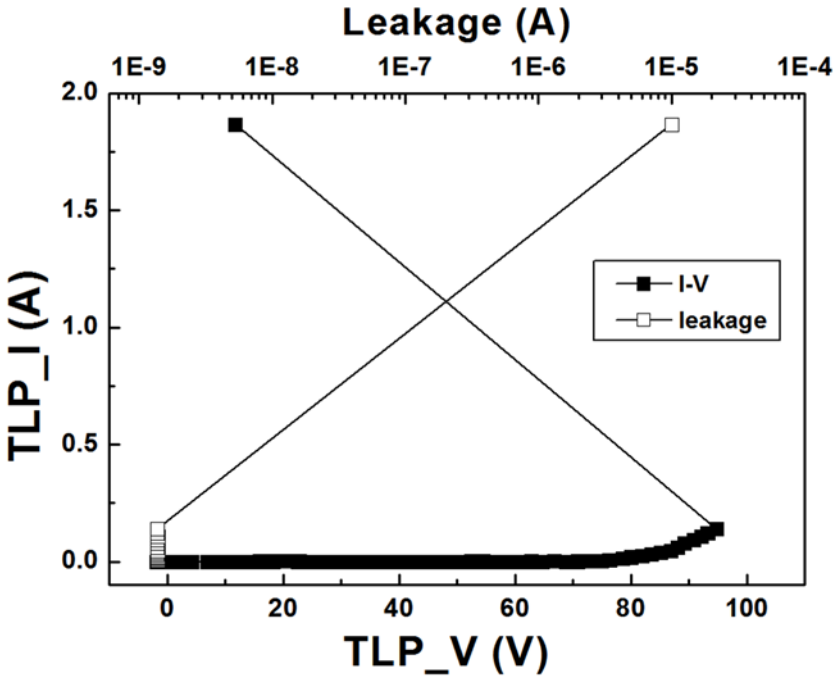

Fig. 3.3 I-V characteristics of standard nLDMOS with minimum rule of all the parameter, which is measured by 100-ns TLP system.

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3.2Parameter Investigation of Stand-alone nLDMOS

There are many different ways to enhance the stand-alone nLDMOS's ESD robustness. Some may change the concentration of the doping profile or adding other different layers to change the electric field or charge distribution [22], [23]. Take the deep drain profile engineering for example, in the deep drain case, a deep n+ sinker was implanted below the drain junction with the same effective drift length of the shallow drain one.The sharply localized temperature increases near the drainjunction was thus avoided. Hence, the ESD level of a deep drain device is higher than the shallow ones [22].The changing layer method is not flexible for applications because the junction depth and concentration is controlled by the foundry. Instead of changing the layer, changing some layout parameter may be another choice.Stretching some parameter of the devices to make the ESD current flow deeper or using a large area to sustain the ESD currentare common techniques in ESD protection design. But

enlarging area need to consider the uniformity issue. To increase the efficiency of ESD performances per micron, embedded SCR structure inside nLDMOS is a popular way to increase ESD robustness. This chapter shows some experimental results for those ideas that have been mention above.

3.2.1 Stand-alone nLDMOS with different total width

The stand-alone LDMOS has poor ESD robustness. To improve the ESD level, the conventional method is to increase the device total width though it would need a large area for ESD protection. There are three kinds of nLDMOS with different total widths are studies in this section (480μm, 800μm and 1120μm, respectively). Those devices are almost the same with the standard cell that foundry gives as a layout samples except that the parameter between contacts to the active region edge. To avoid the large current go through the active region, the space between contacts to the active region has been lengthened to 1μm. Each fingeris 80μm in those devices. So the numbers of three different total widths are 6, 10 and14 respectively. The TLP measurement results are shown in Fig. 3.4.

According to the TLP result in Fig. 3.4, the increasing of the total width does increase the maximum current-handlingability (the secondary breakdown current, It_2). In fact, increasingfour fingers would increase I_{t2} level around 100mA. Also, the resistance of the I-V curve in Fig. 3.4 decreases when the total width increases. For those two reasons, non-uniform turn on may not be the main issue of the stand-alone nLDMOS. But even increasing the total width to 1120μm, the It_2 level is still not good enoughto protect itself. So, enlarge the total width of nLDMOS would not be an efficient wayto get higher ESD level.

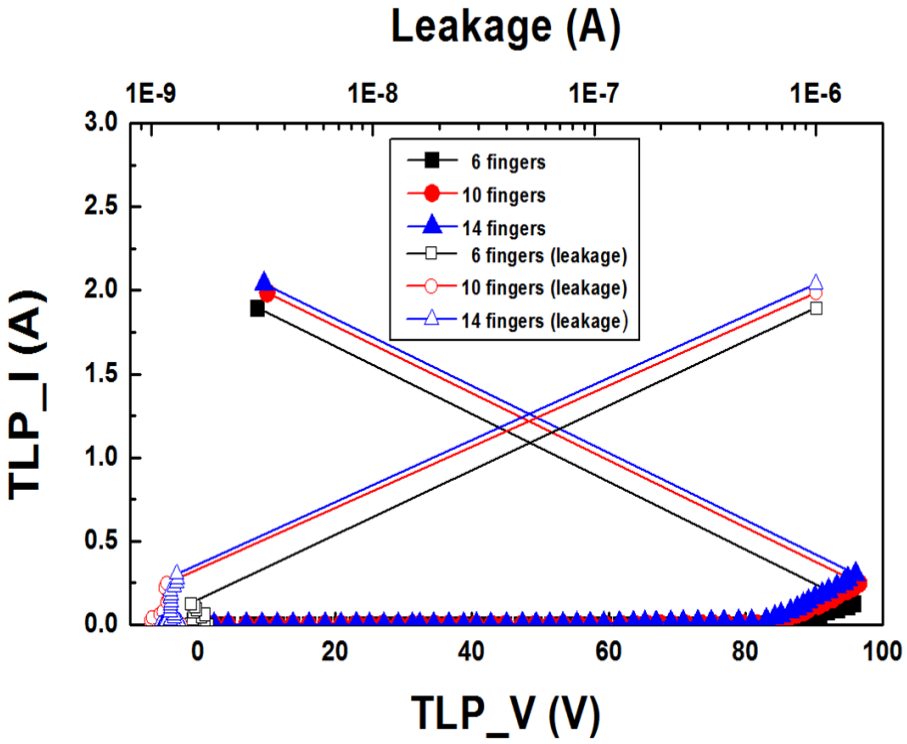


Fig. 3.4 The I-V characteristics of nLDMOS which has different number of fingers. (Each finger is 80μm)

3.2.2Stretchparameter of STI space and drain diffusion region

One way to get better ESD level is to reduce the electric field or local heating in the surface. Drain side engineering is one of the popular ways. Some previous studies use the TCAD simulation to prove that if the isolation between the drain and gate is not large enough, then most current crowded near the surface [10], [24]. Stretching some space in the drain side would let the region, where hot carrier generates, far from the channel. So the currentscan go deeper and more uniform, which also help the parasitic bipolar be triggered[24].

In this section, the parameter of shallow trench isolation (STI) space and drain diffusion region have been studied. Changing the space between active region andthe contactsin the drain side is marked as the parameter d in Fig. 3.5. The TLP results of

different parameter d are shown in Fig. 3.6. The other parameter S of nLDMOS in this case is kept at 3.8μm which is as same as the length of the device in section 3.2.1. There is no significant improvement onESD robustness of nLDMOS with different d according to Fig. 3.6. Then consider the parameter of the STI space, which is markedas the parameter S in Fig. 3.5, Fig. 3.7 and Fig. 3.8 are the measurement results of the three different S (which is 3.8μm, 5.8μm, and 7.8μm, respectively) in different parameter d.Figure 3.9 shows the comparisons of It_2 levels among the single devices under different dand S.When d is 1μm,there has a linear relationship between I_{t2} level and the parameter S. When the d parameter changes to 5μm, the relationship between I_{t2} level and the parameter S also changes. The I_{t2} level does not have large difference when the parameter S is 5.8μm, and 7.8μm. Considering the size and the ESD performance, the device, which d equals to 5μm and S equals to 5.8μm may be the best solution among those six devices. Even though stretchingthe parameter S and d in the sectiondo increase the ESD performance, the device still cannot pass the HBM 2kV level.According to Fig. 3.7 and Fig. 3.8, none of those devices can get into snapback region before it failed maybe the reason. Changing the spacing can delay the damage inthe channel of nLDMOS, but it can't help the device snapbacks. If the device doesn't get into the snapback region, high voltage across the device may cause thethermal damage and resultin the low It_2 levelin 0.25μm 60V process.

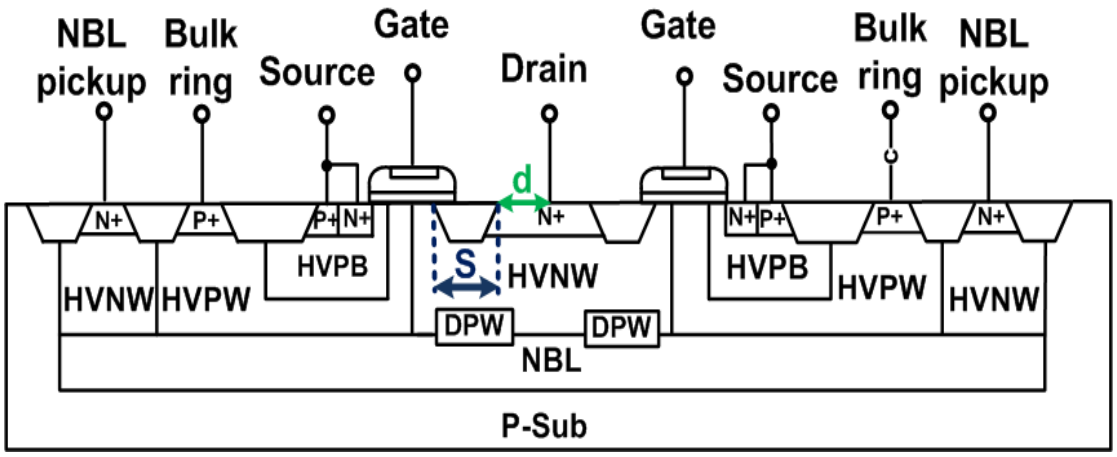


Fig. 3.5 The cross-sectional view of standard nLDMOS in a 60-V BCD process with parameter S and d.

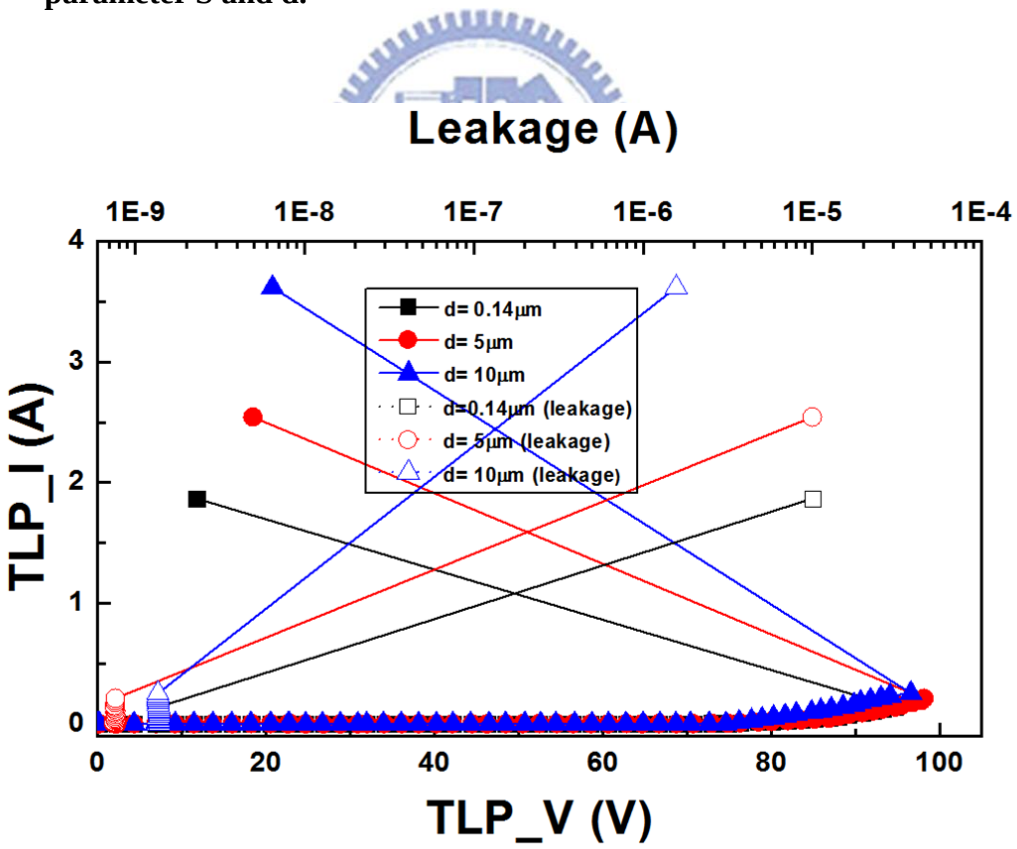


Fig. 3.6 I-V characteristics of nLDMOS with different parameter d. (d=0.14μm, 5μm and 10μm, respectively.)

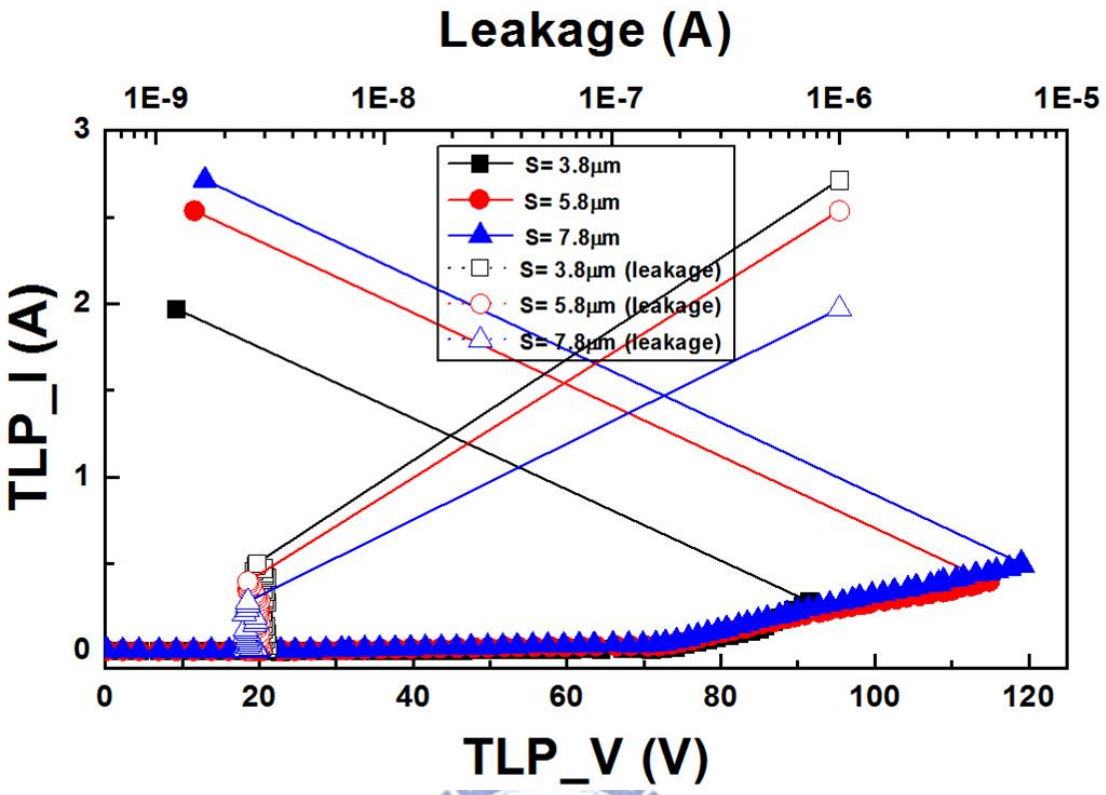


Fig. 3.7 I-V characteristics of nLDMOS with different parameter S (d=1μm).

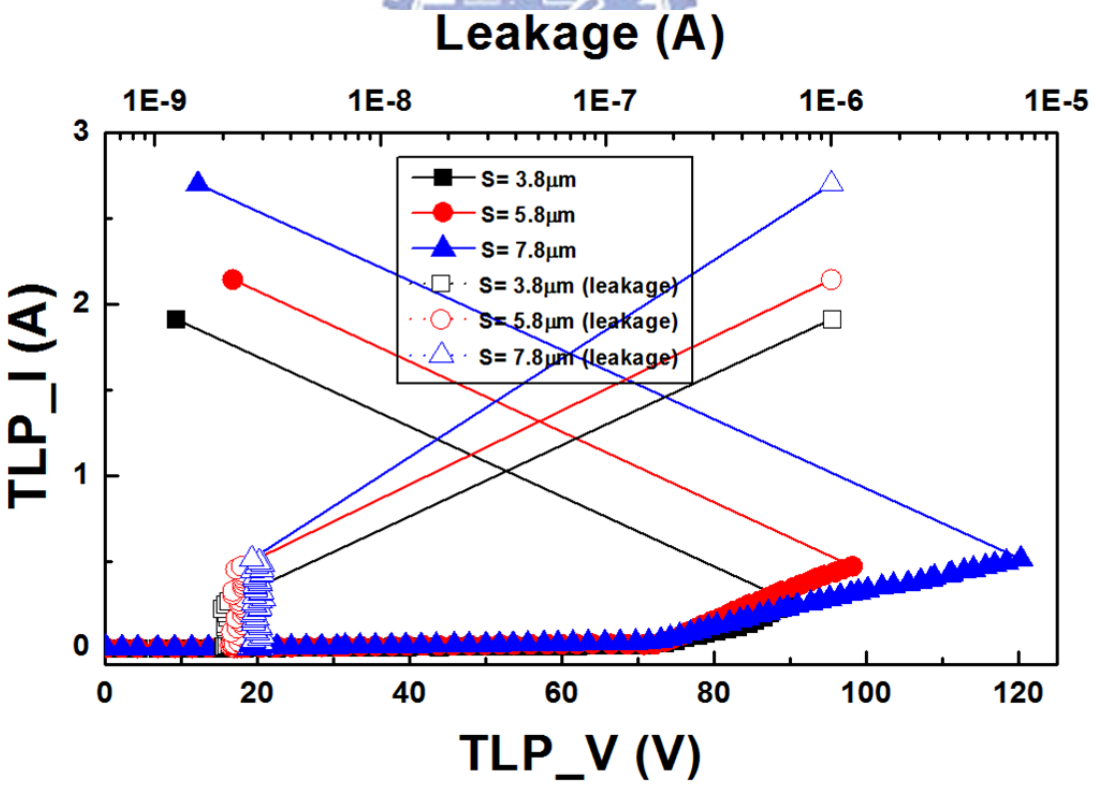


Fig. 3.8 I-V characteristics of nLDMOS with different parameter S (d=5μm).

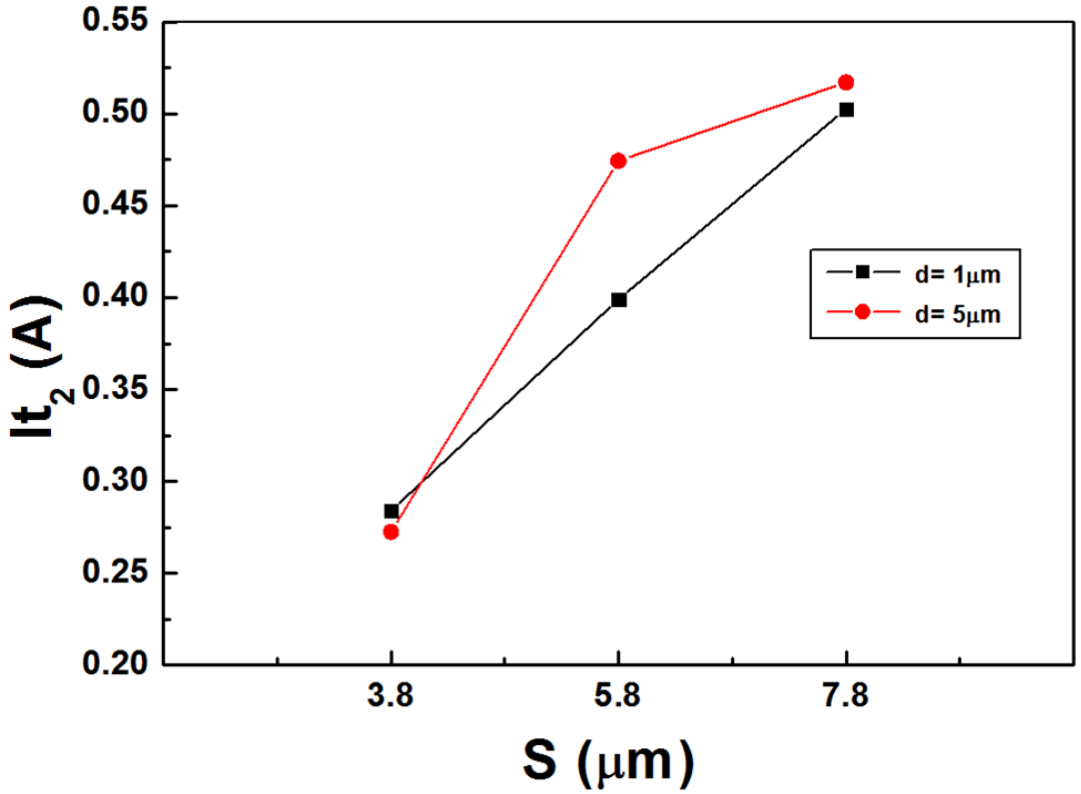


Fig. 3.9 CompareIt_2 levels among the single devices under different dand S.

3.2.3Change the NBL type of stand-alone nLDMOS

The bipolar's unable to turn on and current crowding effects are the rootsthat cause the device failed at the low-voltage ESD zap. Separating the bulk away the source can help the parasitic bipolar be triggered on easier by increasing the parasitic resistance between source and bulk. This method is not good for ESD improvement due to the space between source and bulk should be large enough [10]. Moreover, in reference [24], the most currents flow from drain to NBL underneath and then into source by the TCAD simulation which is shown in Fig. 3.10. Hence, there comes an idea that splitting NBL into little pieces.Changing the shape of NBL can help to control the current distribution. If the device failed because of current crowed, splitting NBL may force the currents distribute more uniformly. There are three types of NBL are studied in this section. The top views of these three types device are

shown from Fig. 3.11 to Fig. 3.13. In Fig. 3.11, the whole device is covered by NBL layer. In Fig. 3.12, the one NBL splits into four fingers with the minimum space between two fingers. Moreover, there are eight NBL fingers in Fig. 3.13.The spacesbetween two fingers are kept in the minimum rule. The TLP measurement results of these three types of NBL with different STI spaces are shown in Fig. 3.14, Fig. 3.15 and Fig. 3.16, respectively.

Comparing the trigger voltage (Vt_1) of three different types of NBL is shown in Fig. 3.17. With fully isolated NBL, the device has the lowest trigger voltage.The trigger maintains the same with different parameter S. No matter how many fingers that NBL splits into, the trigger voltage of these two cases areboth higher than that of the full isolation in the same parameter S. Splitting one NBL layers into many fingers can change the devices' trigger voltage. In other words, changing the layout style of NBL can change the devices' triggering point. Non-fully isolate NBL can have a higher trigger voltage which may have better SOA and more weakly snapback. Fig. 3.18 indicates the comparison of maximum current handling ability (It_2) of three different types of NBL. The It_2 current reduce with the finger increased. The number of the fingers increases means the total area cover by NBL layer decreases. Through this experimental result, splitting the NBL into little pieces can't improve the ESD level. To improve the ESD performances, more investigations are needed.

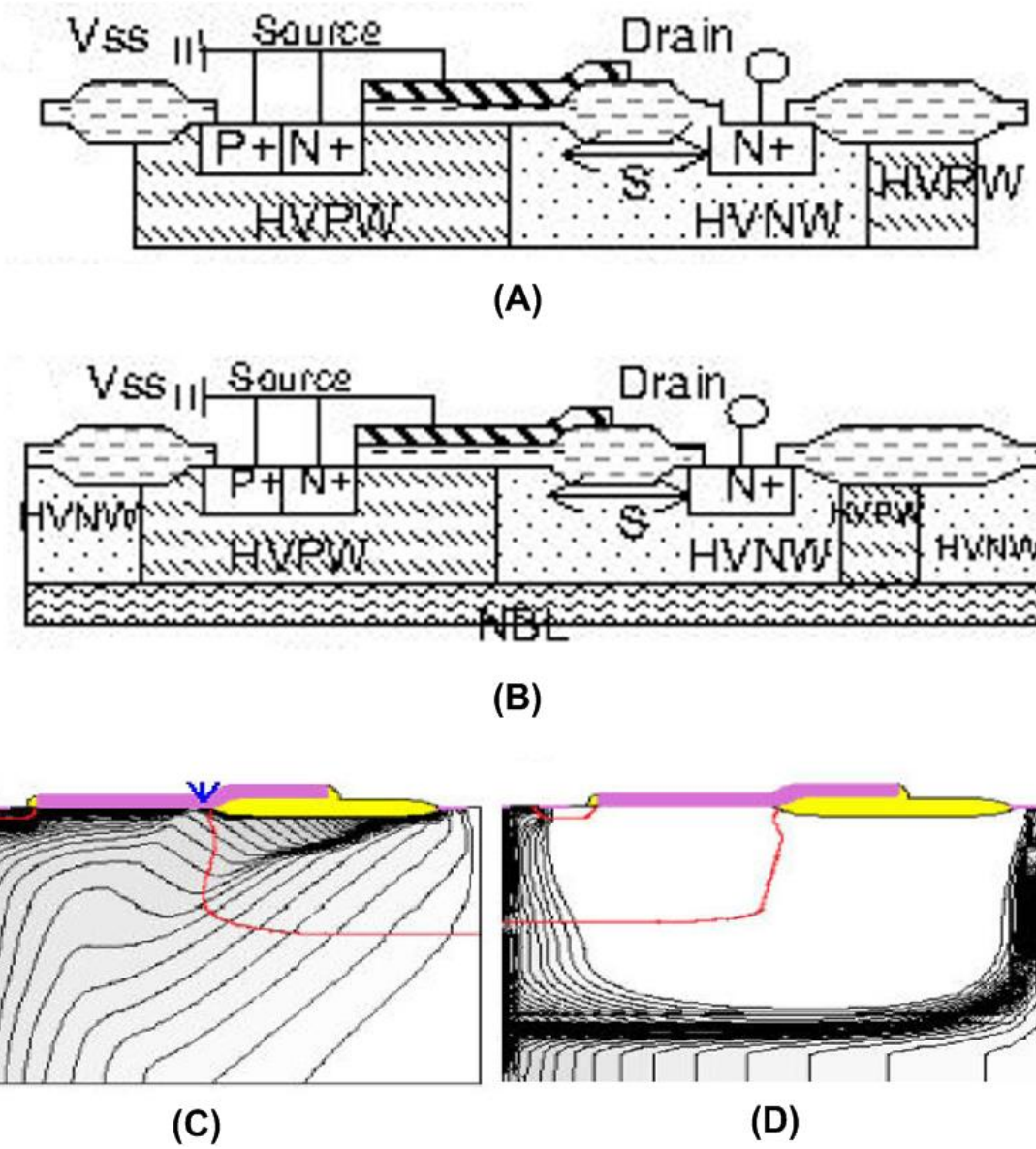


Fig. 3.10 (A) and (B) Cross-sectional view of LDMOS (S=5μm) in 40V process without and with isolate NBL.

(C) The current flow contours of LDMOS without NBL.

(D) The current flow contours of LDMOS with NBL.[24]

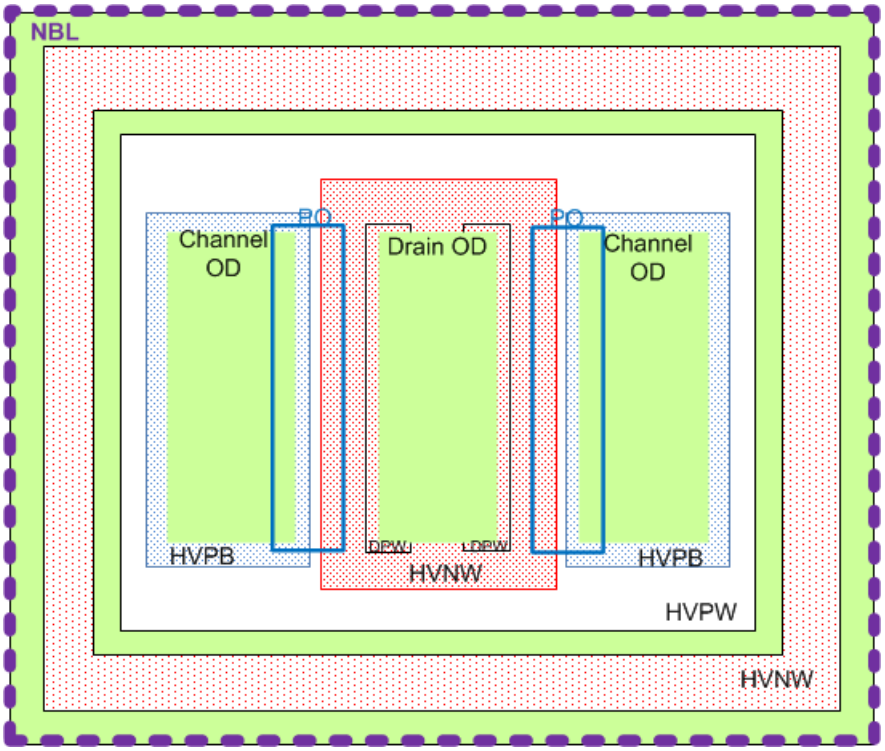


Fig. 3.11 The top view of nLDMOS which is covered by one NBL layer (Type 1).

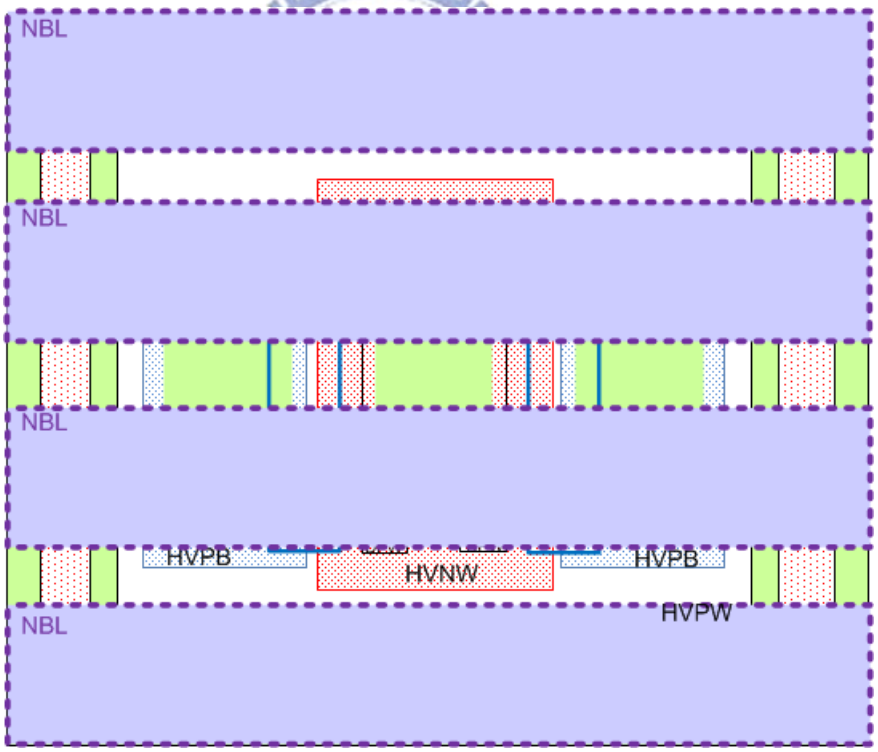


Fig. 3.12 Thetop view of nLDMOSdevice which is covered by four NBL fingers (Type 2).

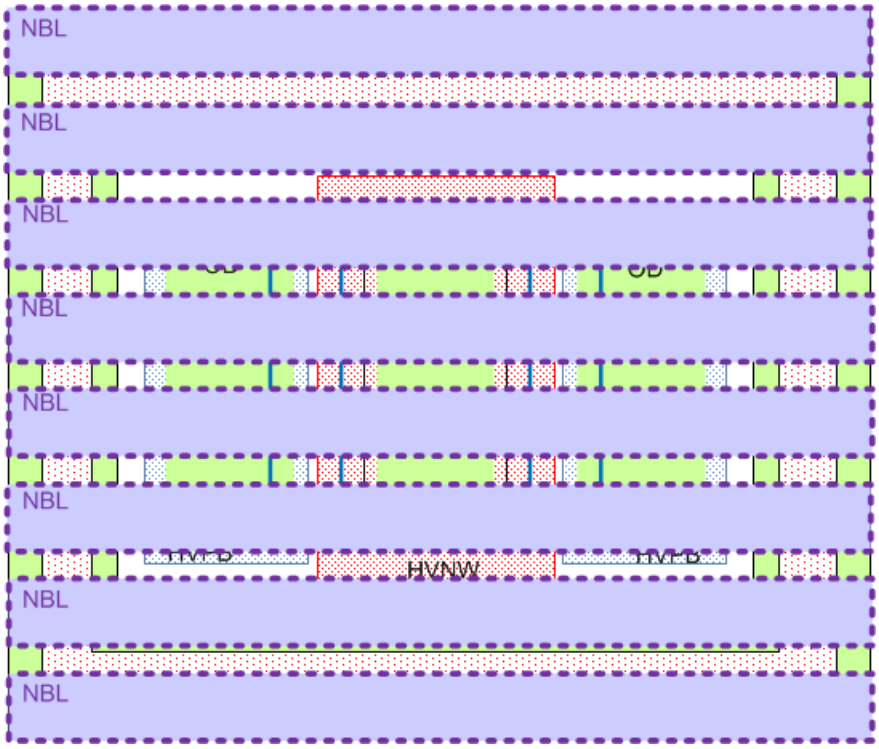


Fig. 3.13Thetop view of nLDMOS device which is covered by eight NBL fingers (Type 3).

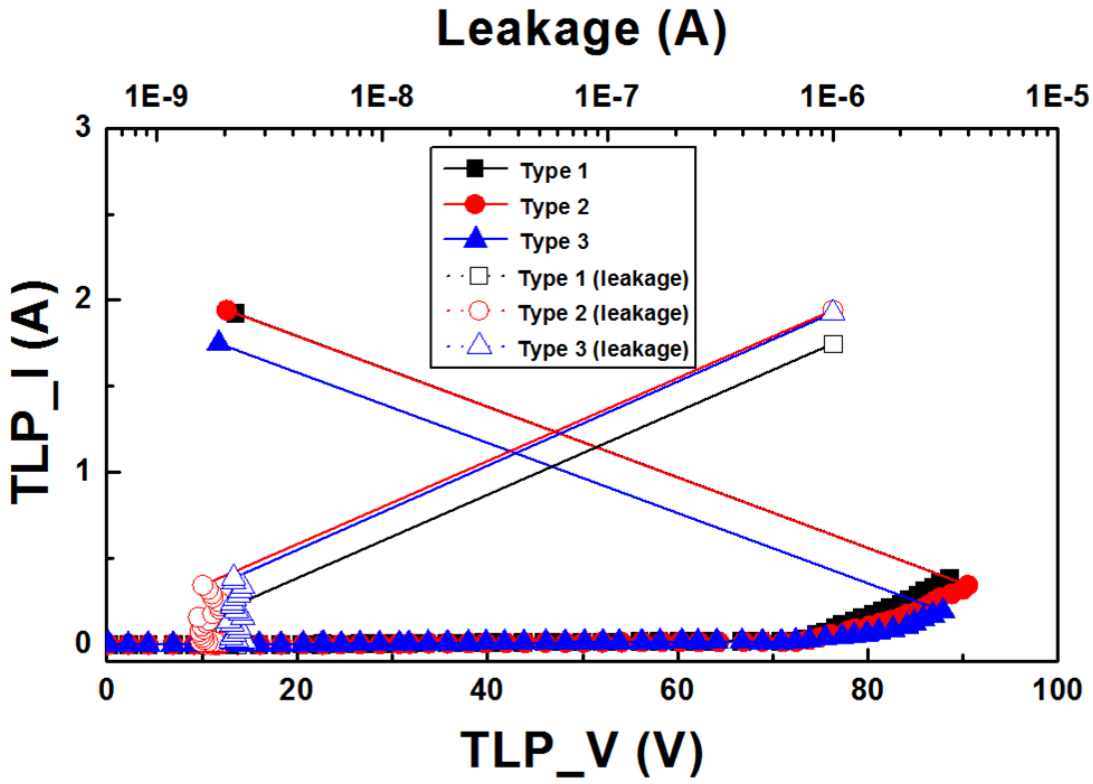


Fig. 3.14 The TLPresults of the deviceswith three types of NBL. (The space of STIis 3.8μm).

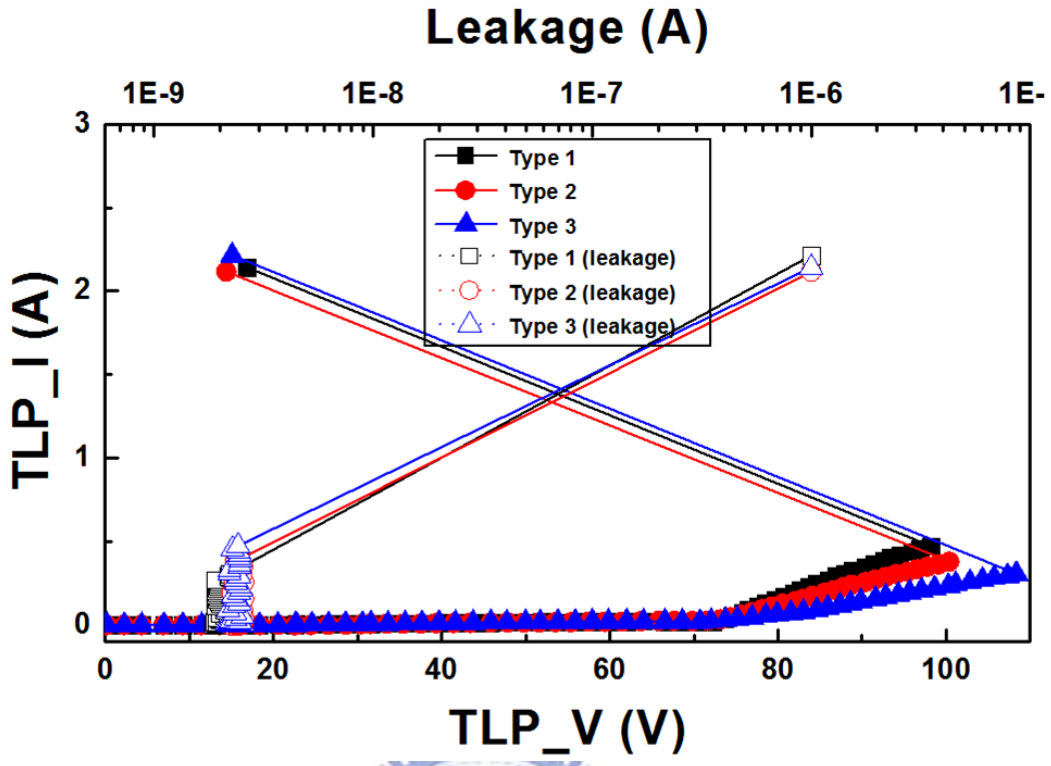


Fig. 3.15 The TLP results of the devices with three types of NBL. (The space of STI is 5.8μm).

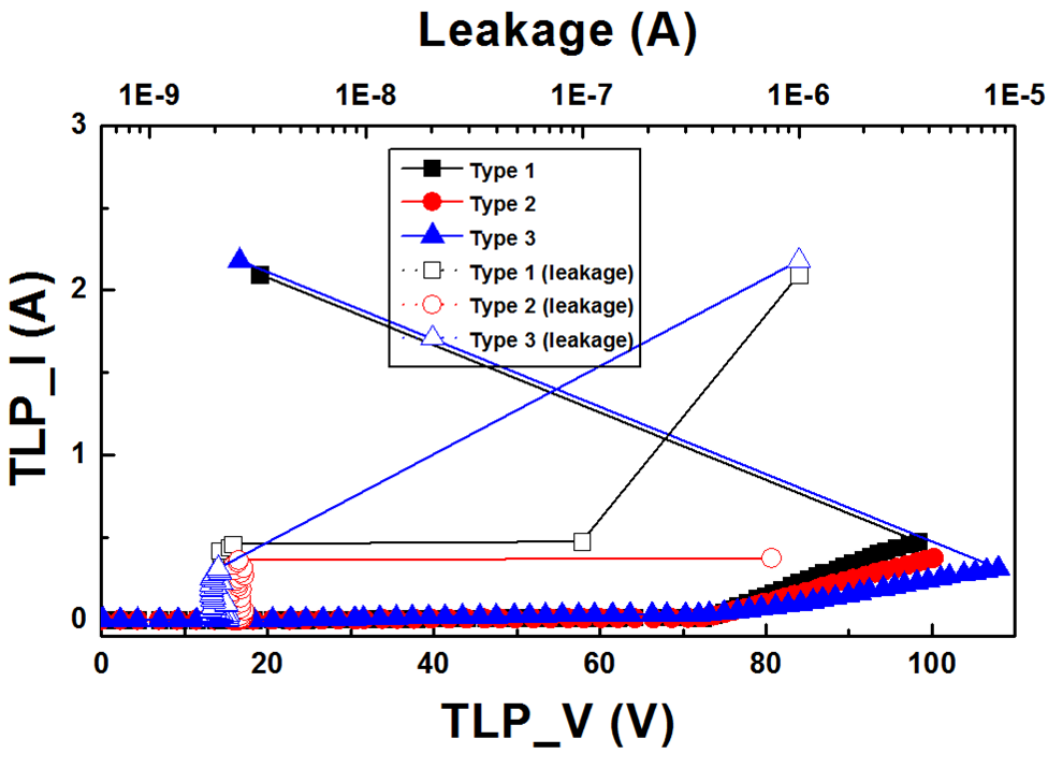


Fig. 3.16 The TLP results of the devices with three types of NBL. (The space of STI is 7.8μm).

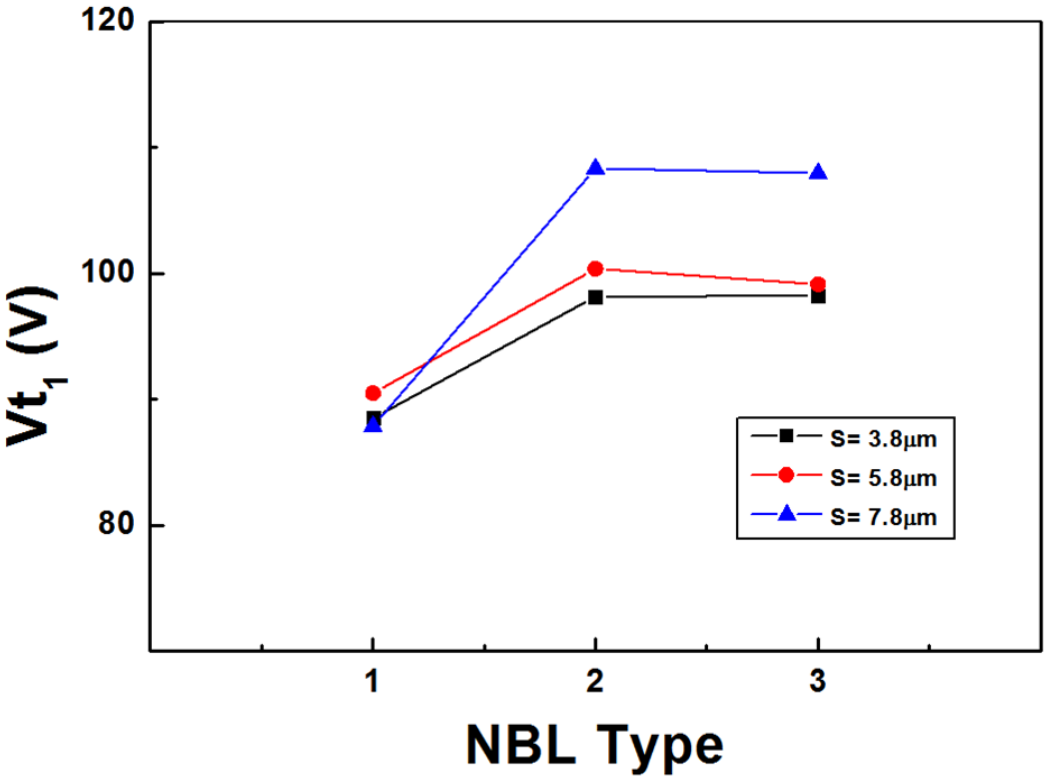


Fig. 3.17 Compare the trigger voltage (Vt_1) of three different types of NBL.

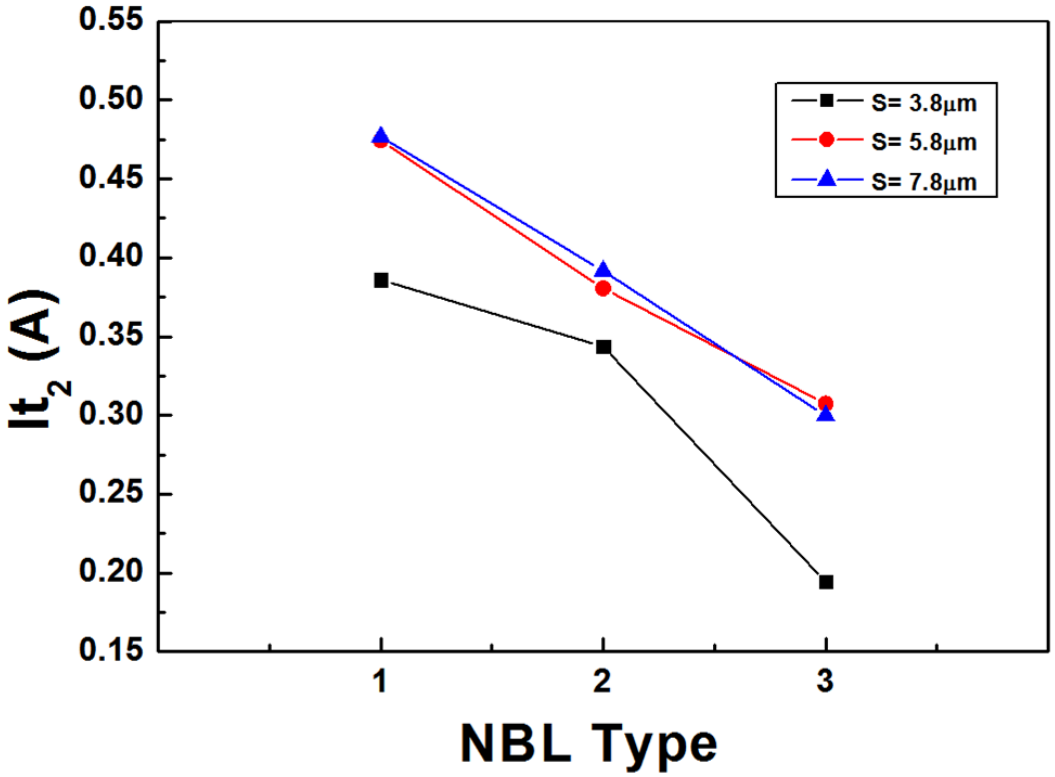


Fig. 3.18 Compare the maximum current handling ability (It_2) of three different types of NBL.

3.3 Investigation on Different Typesof Embedded SCR in nLDMOS

3.3.1 Embedded SCR structure in stand-alone LDMOS

There are several solutions proposed to increase the ESD robustness of nLDMOS. The most popular way to improve ESD robustness is inserting silicon controlled rectifier (SCR) into the LDMOS [25],[26]. SCR is known as an area-efficient method to improve ESD robustness. But it may have higher trigger voltage than that of stand-alone LDMOS. Under ESD stress, since the stand-alone nLDMOS cannot be triggered with many different parameter and different layout style which has been reported in section 3.2, the embedded SCR LDMOS will fail before the embedded SCR is triggered on to discharge ESD current. The following work combines the concepts of changing thelayout space and embedded SCR inside LDMOS todevelop some new structure of self-protected LDMOS

3.3.2 Adding more implant layer in the source side

The bipolar's unable to turn on and current crowding effectsare the roots of the HV-LDMOS failed at the low-voltage ESD zap.If the two causescan be eliminated, the ESD performance of the HV-LDMOS willbe improved.To decrease the trigger voltage, several ways, such as increasing the emitter space and adjust the well/substrate resistance of the MOS, had been studied in previous work.

Although separating the bulkawaythe source can increase the resistance,the ESD performance of the device still cannot be improvedif it does not haveenoughspacebetween source and bulk[10]. In this process, the high doping concentration of HVPB layer maybe the critical reason that cause parasitic BJT cannot turning on. Therefore, source side engineering can be considered. Fig. 3.19 is the embedded SCR structure with a larger space between source contact and gate. This structure is named S-pn-ref. Increasing the resistance between the substrate and

bulk by increase the space from source contact to HVNW edge may be a good solution for helping the parasitic bipolar be triggered. Fig. 3.20 is a new proposed structure, named S-pn. This device has an additional p+ and n+ implant between the source contact and gate. The total area that device occupied of those two structure are the same. On the other hand the space between source contact and gate, which is the parameter A is remain the same. Fig 3.21 and Fig. 3.22 compare those two structures with different S. Though in Fig. 3.21, two devices are not snapback before the device failed. But when the parameter S is large enough (S=5.8μm), the S-pn-ref can get into a snapback region successfully (Fig. 3.22). Adding more p+ and n+ implants would let the device more difficult to be triggered. This argument will be discussed particularly in a more simple structure in chapter 4.

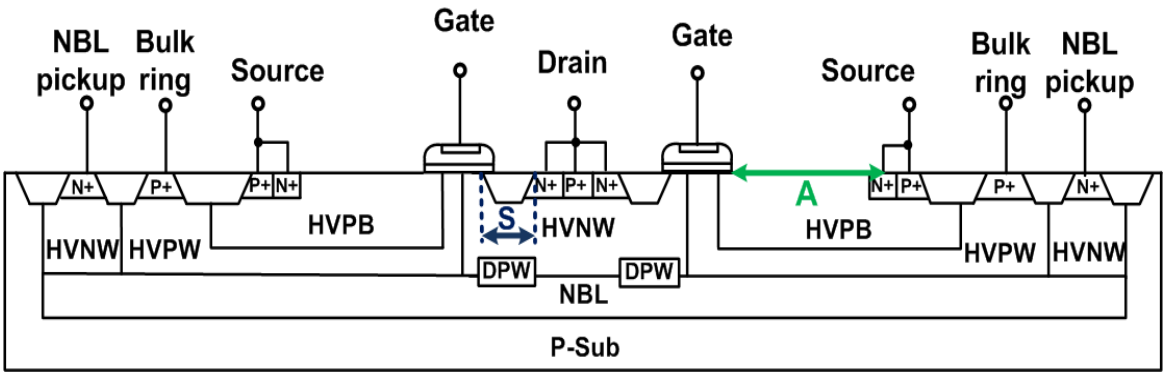


Fig. 3.19 The cross-sectional view ofembedded SCR structurewith larger parameter A in a 60-V BCD process (S-pn-ref).

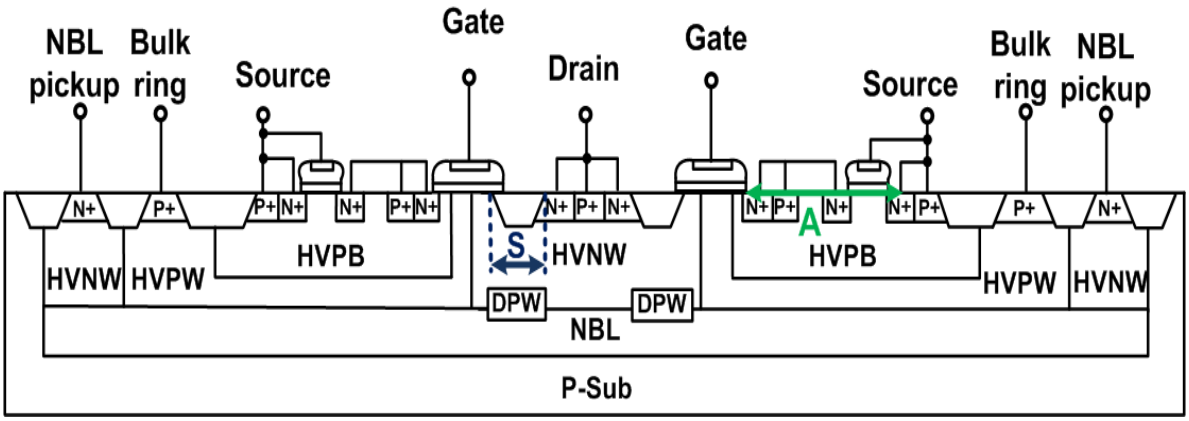


Fig. 3.20 The cross-sectional view of new proposed embedded SCR structurewith source side engineering in a 60-V BCD process (S-pn).

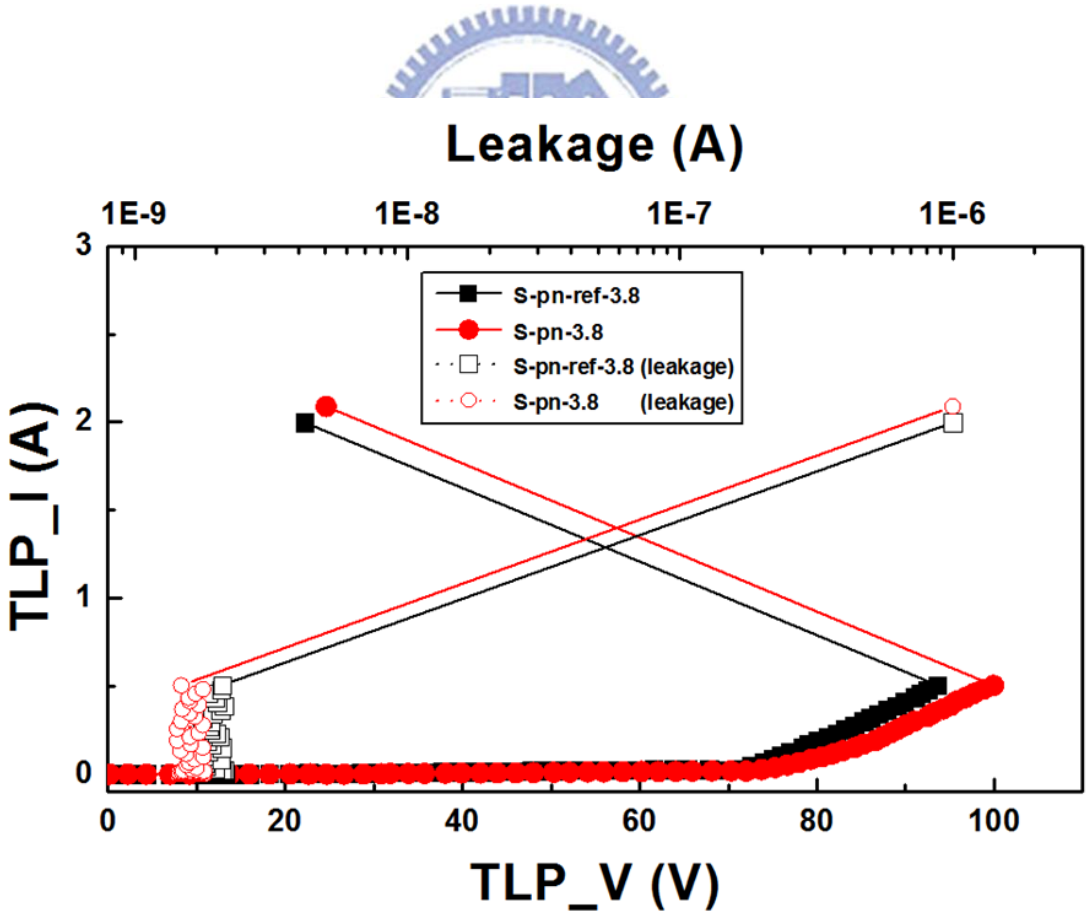


Fig. 3.21 The TLP results of S-pn-ref and S-pn. (The space of STI is 3.8μm).

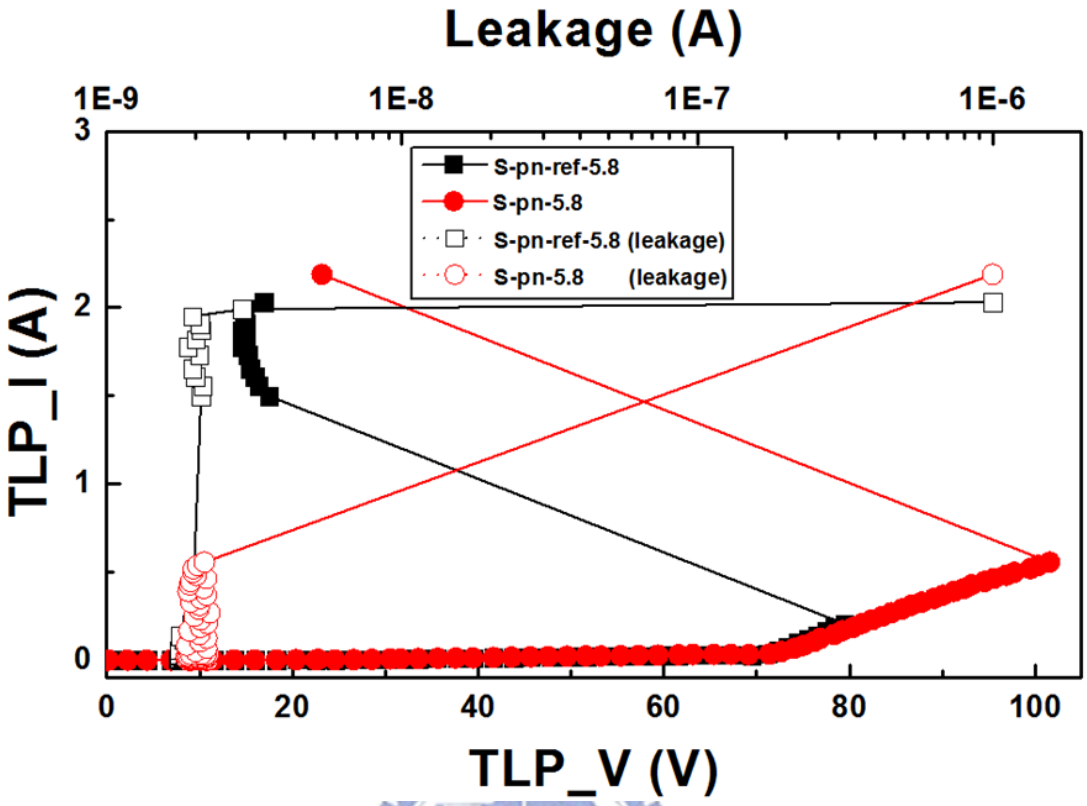


Fig. 3.22 The TLP results of S-pn-ref and S-pn. (The space of STI is 5.8μm).

3.3.3 Adding more implant layer in the drain side

The drain-side engineering has attracted many people to research HV devices recently. It prevents the kirk effect and avoids reliability problem[22],[27]-[29]. Somestudies indicate that higher dosage can improve the reliability of nLDMOS transistors. Also, the junction depth increasing in the drain-side will result in the higher holding voltage of an nLDMOS[30]. Some of them report that filamentation can be avoided in conventional LDMOS structure in the snapback region when the ballast resistance during snapback is large enough.During the experimental results of the nLDMOS device in 0.25μm 60V BCD process in section 3.2.2, only stretching the layout parameters in drain region can’ttrigger on the parasitic bipolar junction, not to mention the embedded SCR structure. Fig. 3.23 is named LDMOSSCR, which is modified from LDMOS byinserting p+ implantation region in drain active region

tocreate the parasitic SCR path. Also rearrange the implant order to meet the DRC rule. EmbeddedSCR inside LDMOS is the simplest way to improve ESDlevel if the parasitic device can betriggered on before it failed.Both stand-alone LDMOS and embeddedSCR structure failed before snapback in this high voltage process, so thecurrent-handling ability of those two devices isvery low. Besides, the breakdownvoltage of the embedded SCR LDMOS is down to 59V,which is lower than the maximum supply voltage of 60V.The reason of this phenomenon may be the increasing of minority carrier. The p+ implantation provide some hole in the drain side in the embedded SCR structure. The punch through of the hole may result in the lowering of the breakdown voltage and make the device can't be used in the normal situation.

Fig. 3.24 is a new proposed structure inserting more n+ and p+ implant layers between the gate contacts and STI. In this structure, there is adummy gate between two p+ regions for reducing thetotal space and increasing the gain of the parasitic BJT.To make sure that the parasitic pMOS being kept off, thedummy gate is connected to the drain. The new proposed structure is fully process compatible to high voltageprocess without additional mask layer or process step.Those two structures have the same parameter B. The TLP measurement results of drain engineering in different parameter S is shown in Fig. 3.25 and Fig. 3.26, respectively. When the parameter S is equal to 3.8μm, there is no notabledifference between drain-extend nLDMOS and the new proposed one. But when the parameter S is 5.8μm, the new proposed device sometimes can be triggered on. The I-V curve in Fig. 3.26 indicates thatnew proposed structure can be triggered on around86V and get into the snapback region.Separating the space of additional p+ and n+ implantation layers would let the device get into snapback region stably. The device that additional p+ layer is close to the n+ layer (which the parameter k=0μm)is called D-pn-kmin. The device with

separating p+ layerand n+ layer (which the parameter k≠0μm) is called D-pn-k5.This optimized structuresuccessfully reduces the trigger voltage by doing those drain engineering.Consequently, it has a higher It2 (> 2A) than others. Moreover, the breakdown voltage of this device maintains in 75V,which is similar to the stand-alone LDMOS. This device can be used as a self-protected ESD device in 60 V circuit. The HBM robustness of the new proposed device is also improved. The measurement result of the stand-alone LDMOS is 1.5kV. The news structure can pass more than 2kV level which is the best one among these three devices investigated in this work.

There are two ways to explain the improvement in the new proposed structure. First, the current path of the new proposed structure wouldgo deeper than the LDMOS-SCR. Because the NBL is higher doping concentration layer compare with HVNW. The deeper of current distribution would results in the larger total current. Those current would let the parasitic BJT be trigger easier and faster. The more time or energy that the device needed to snapback the more easily result in unrecovered thermal failure. That prevents the new proposed structure failed before the parasitic BJT path has been triggered on. On the other way, the new proposed structure would increase the ESD robustness by reducing the surface electrical field. When inserting the p+ implant layer in the drain side, there would form a neutral region in the interface between p type and n type doping. This region can also avert the electrical field to distribute more vertically.High surface electrical field may stress the gate oxide and cause the unrecoverable damage. These physical understandings can explain the reason why the new proposed structure successfullysnapback and having better I_{t2} levels when comparing to other devices. Plus the modulation of the parameter k, the device named D-pn-k5-5.8 has better ESD levelamong other devices in this chapter.

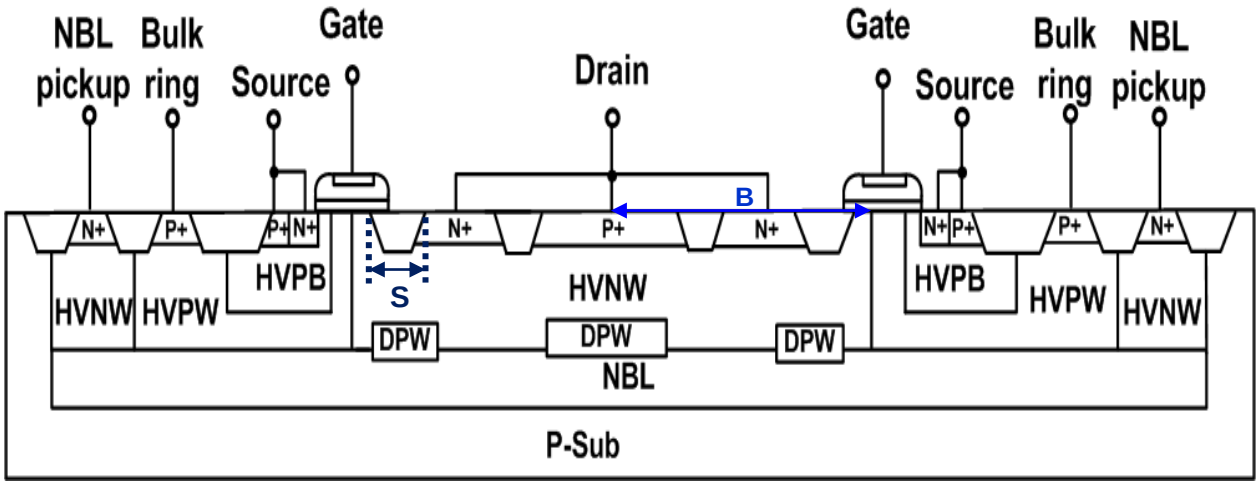


Fig. 3.23 The cross-sectional view ofembedded SCR structure in a 60-V BCD process (LDMOSSCR).

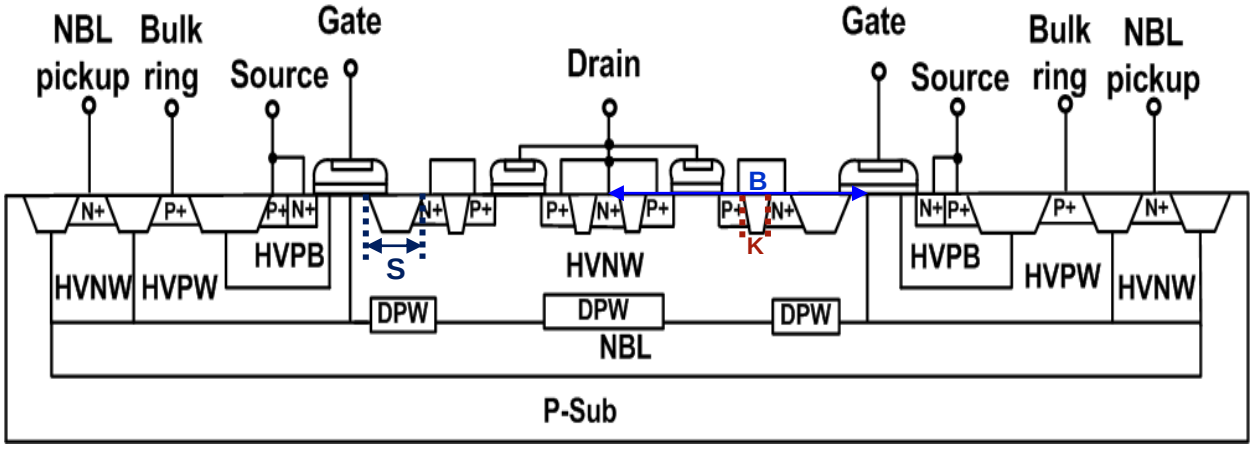


Fig. 3.24 The cross-sectional view of new proposed embedded SCR structurein the drain sidein a 60-V BCD process (D-pn-kmin and D-pn-k5).

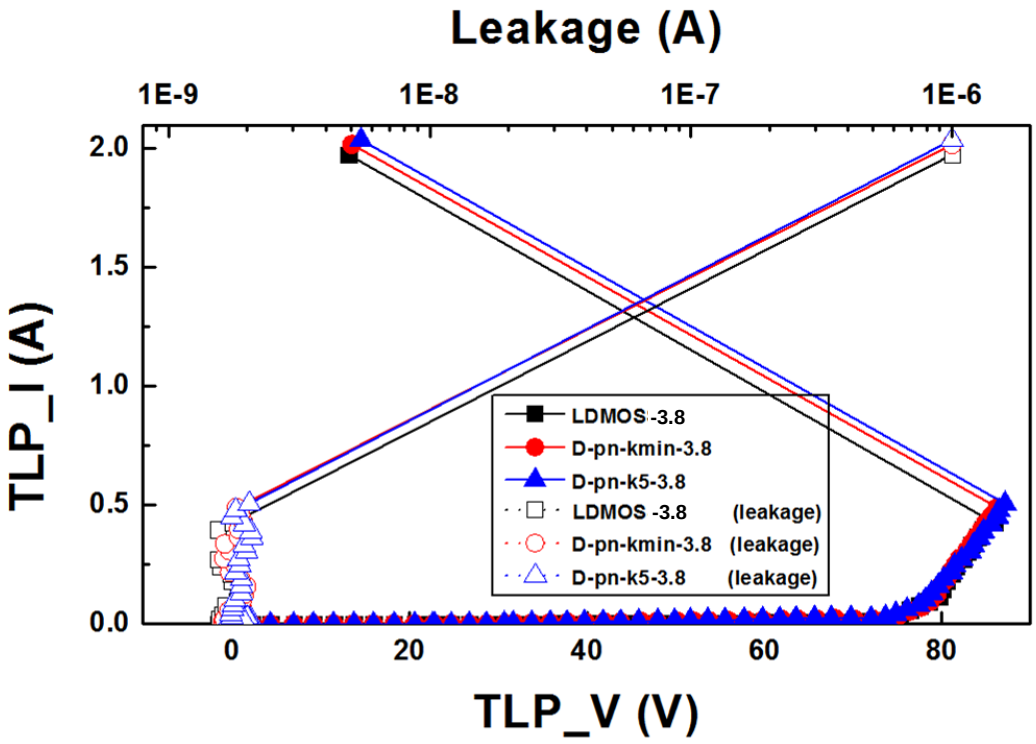


Fig. 3.25 The TLP results of three different type of device with drain-side engineering. (The space of STI is 3.8μm).

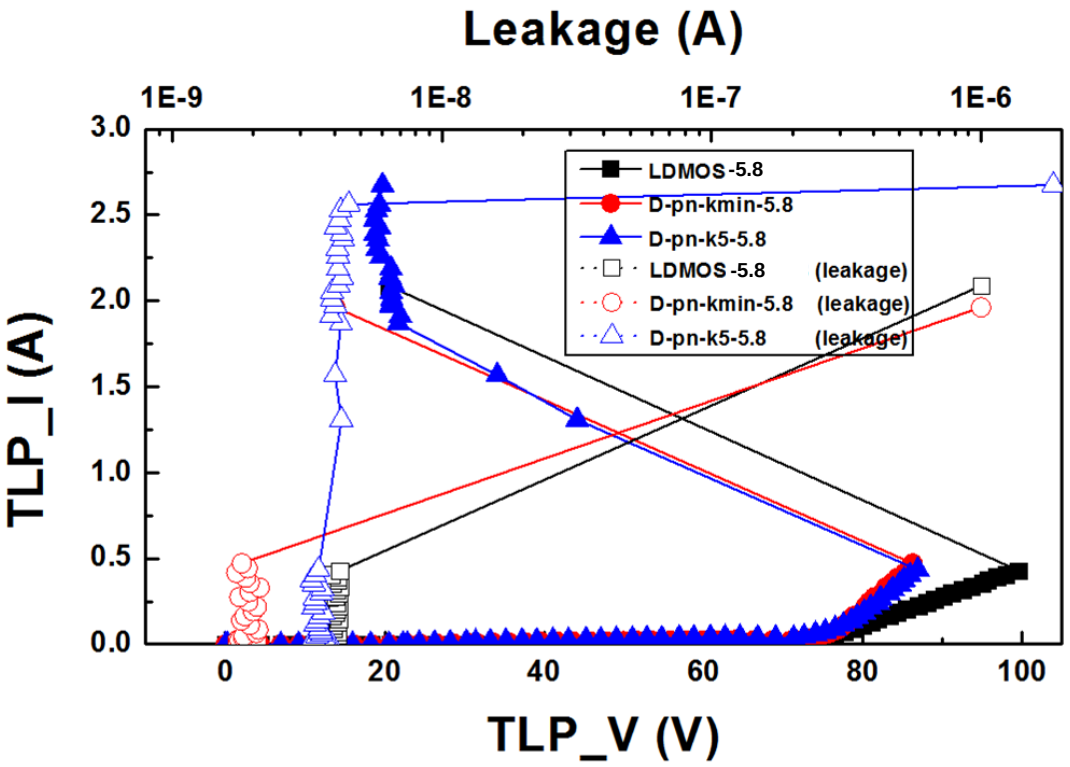


Fig. 3.26 The TLP results of three different type of device with drain-side engineering. (The space of STI is 5.8μm).

3.4 Discussion and Summary

3.4.1 Discussionand failure analysis

In this work, the parasitic BJT of 60-V nLDMOS still cannot be triggered on even ifthe space of STI or the space between the drain contacts to gatestretches. The detail of the experimental results of parameter S and d have been summarized in Table. 3.1. The ESD levels included It_2 and HBM levels have a little bit improved. Because NBL is a highly doping N-type layer, which constructs a low impedance current path to shunt the ESD current through the vertical NPN BJT,changing the layout style of NBL causes different trigger voltage without changing the device breakdown voltage. Because those devices with different type of NBL can't get into the snapbackregion, the It_2 level decreasesas the trigger voltage increases. That is, the total slot area of NBL and the It_2 level are roughlyininverse proportion. However, stretching the source active region would turn on the parasitic bipolar junction when S is enough large. Plus some additional implant layer between the source and gate will increase its trigger voltage in both S cases.

Even though stretching the space between drain contact and STI cannot let the parasitic BJT or SCR turn on, new proposed structure with large parameter S and drain side engineering can get into the snapback region before it failed. Consequently, it has a higher It_2level than others. Thebreakdown voltage of the new proposed structure, which is embedded SCRin LDMOS with larger STI space (named D-pn-k5-5.8),is75V.That device maintains the same breakdown voltage as the stand-alone LDMOS (named LDMOS-5.8) in the same conditions (S=5.8μm, d=5μm).The human-body-model (HBM) ESD robustness of thefabricated devices are all characterized by the ESD tester. Themeasurement result of the stand-alone LDMOS is 1.5kV.The embedded SCR structure only passes 1kV during theHBM test. The new proposed LDMOS-SCR(named D-pn-k5-5.8) can passmore than 2.5kV level

which is the best one among thesethree devices investigated in this work. The failure analysis can also prove those physical understandings, which are mentioned in the last section.The SEM pictures of the embedded SCR LDMOS (LDMOSSCR-5.8) andthe new proposed LDMOS-SCR (named D-pn-k5-5.8) structure after HBM testare shown in Fig. 3.27 and Fig. 3.28, respectively. In Fig. 3.27, thedamage isn't obvious comparing to Fig. 3.28. This phenomenon may result from the low failure current.Conversely, the failure locations afterHBM stress on the new proposed LDMOS-SCR is clearanduniform. Every finger has ESD damage inFig. 3.28. The uniform ESD dissipation current causes theincrease of the self-protection ability of the new proposedLDMOS-SCR during the ESD test.

All theexperimental results are summarized in Table 3.2. The total width of each nLDMOS device in this chapter is 800 μm except the section 3.2.1.

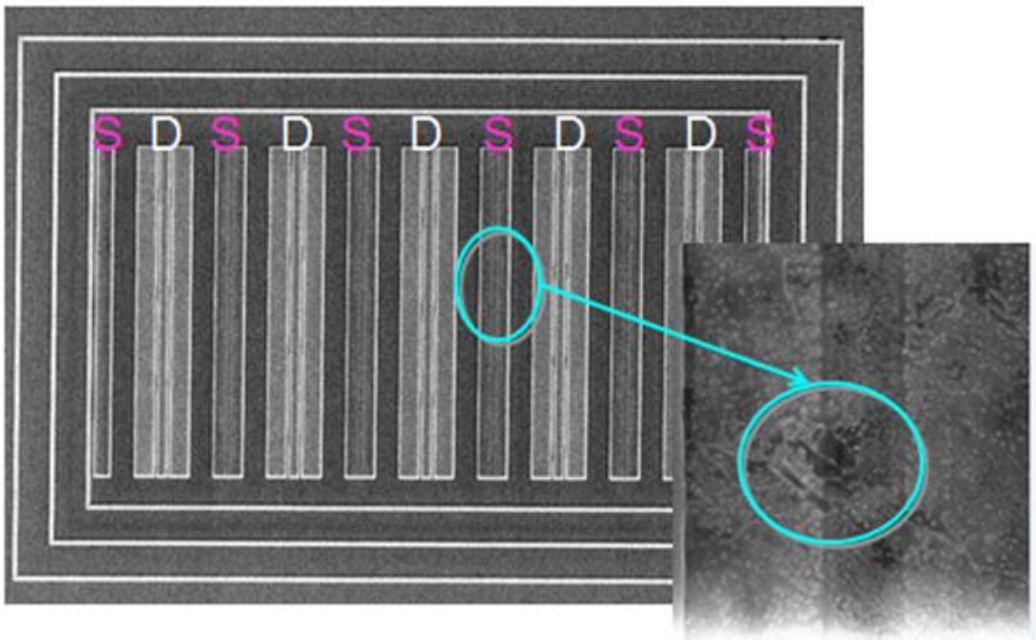


Fig. 3.27 The SEM image of embedded SCR LDMOS device (named LDMOSSCR-5.8) after 1.5kVHBM test. (S=5.8μm case)

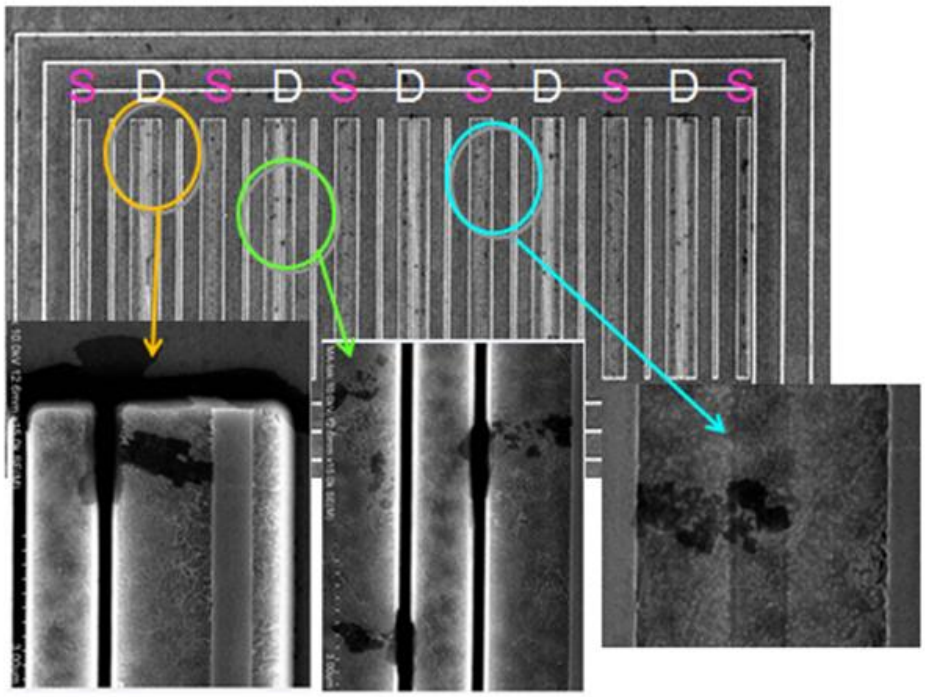


Fig. 3.28 The SEM image of new proposed device (D-pn-k5-5.8) after 2.5 kVHBM test. (S=5.8μm case)

TABLE 3.1

Summarize the ESD robustness of nLDMOS devices with different S and d.

		d=1 μm	**d=5 μm**
S=3.8 μm	Breakdown voltage (V)	75 V	75 V
	Trigger voltage (V)	91 V	88 V
	It_2 level (mA)	278 mA	378 mA
	HBM (kV)	0.5 kV	0.5 kV
S=5.8 μm	Breakdown voltage (V)	75 V	75 V
	Trigger voltage (V)	114 V	96 V
	It_2 level (A)	404 mA	480 mA
	HBM (kV)	0.5 kV	1 kV
S=7.8 μm	Breakdown voltage (V)	75 V	75 V
	Trigger voltage (V)	119 V	96 V
	It_2 level (A)	510 mA	472 mA
	HBM (kV)	1 kV	1.5 kV

TABLE 3.2

The TLP-measured results and ESD robustness with different embedded SCR devices

Device name	Breakdown Voltage	Trigger Voltage (Vt_1)	Holding Voltage (V_h)	It_2 Level	HBM
S-pn-ref-3.8	73 V	78 V	none	200 mA	< 0.5 kV
S-pn-3.8	74 V	93 V	none	505 mA	1 kV
S-pn-ref-5.8	74 V	79 V	14.5 V	1.8 A	2 kV
S-pn-5.8	74 V	101 V	none	556 mA	1.5 kV
LDMOS-3.8	75 V	86 V	none	378 mA	< 0.5 kV
D-pn-kmin-3.8	75 V	86 V	none	460 mA	0.5 kV
D-pn-k5-3.8	75 V	86 V	none	507 mA	1 kV
LDMOS-5.8	75 V	87 V	none	480 mA	0.5 kV
D-pn-kmin-5.8	75 V	87 V	none	430 mA	1 kV
D-pn-k5-5.8	75 V	87 V	22.7 V	1.9 A	2.5 kV

3.4.2Summary

The test devices for study of self-protected HV MOSFET have been investigated in a 60-V BCD process. One of the conventional methods to enhance the ESD robustness of stand-alone LDMOS is to increase the device's total width. But in this 60 V process, even though the total width increases to 1120μm, the HBM level of

nLDMOS is still only 0.5kV, which is far away from the specification (2kV). According to the measurement results, increasing the total width is not an efficient way to improve the ESD performance. Non-fully isolate NBL can have a higher trigger voltage which may have better SOA and more weakly snapback. If the device successfully snapback, changing the layout style of the NBL may modify the trigger point to meet the application.In this process, the nLDMOS cannot get into the snapback region by changing the layout style of NBL. Changing the parameter of STI space and drain contacts to STI region can only let the device bear more heat. Those devices with larger S and d may have the unrecoverable thermal damaged in the higher TLP step. However, only changing the parameter of STI space and drain contacts to STI region still cannot trigger the parasitic junction. Increasing the source active region may help the parasitic device turning on. The larger space between source contacts to the polygatewould decrease the trigger voltage. Adding additionalp+ and n+ layersin source side would let the parasitic SCR become difficult to be triggered or even unable to snapback. This concept would be discussed in the next chapter.

Many previous works havedone some engineering in drain for improve ESD robustness.The new proposed structure (D-pn-k5-5.8) is based on the embedded SCR in nLDMOSwith large parameter S and d. This device can get into its snapback region successfully. Hence, this device not only increases its It_2level to more than 2A but also improves the HBM levelto over 2.5kV, which can meet the typical ESDspecification of commercial IC products. Besides, this structure (D-pn-k5-5.8) keeps the same electrical safeoperation area due to the breakdown voltage unchanged.The new proposed LDMOS-SCR structure, which is namedD-pn-k5-5.8, will be theuseful self-protection solution against ESD events inhigh-voltage applications.

Chapter 4

Modification for LVSCR and HVSCR Structure

4.1Embedded SCR structure in 60-V 0.25 μm BCD Process

As mentioned in Chapter 3, nLDMOSdid nothave enough self-protected abilityto againstESD stresses.Therefore, an additional ESD protection designisneeded in HV applications.To simplify the HV device and remove the gate oxide damage issue, many different SCR structures are studied in this chapter. During the ESD condition, the leakage current of SCR flows deeper to prevent the current crowed effect. So it becomes one of the popular ESD protection devices in HV process.

This work not only uses the concept of layers investigation and stretching the layout parameters but also combinesthe new proposed technique by adding additional n+ and p+ layers and Schottky emitter method to increase the holding voltage of SCR. Those ESD protectiondevices have been proposed in a 0.25-μm 60-V BCD process. The detail of those devicesstructures and ESD performances will be introduced in the following.

4.1.1 Investigation for layer effect upon the SCR structure

In this chapter, all device inserting p+ implantation in the anode side to create the PNPN (P+-HVNW-HNPW-N+) SCR path for ESD robustness improvement.Fig. 4.1 shows thecross-sectional view of simple SCR structure (which is named HVSCR). This device's breakdown voltage is controlled by the junction of HVNW and HVPW.After the junction breakdown, the leakage currents flow through HVPW and create a voltage drop between the HVPW and N+ node in cathode. When the voltage

across HVPW and N+ node in cathode is large enough to turn on the parasitic NPN BJTjunction, the parasitic PNP BJT will be turned onat the same time. The positivefeedback of those two BJTs in SCR is the reason why SCRcan have such low holding voltage. For latchup immunity, the second device, named HVSCR+SH_P, add some higher doping layers (SH_N and SH_P) trying to adjust the effective doping concentration of the parasitic BJT junction. More highly doping layer may let the SCR is more difficult to turn on, so that the holding voltage of the SCR may increase.

In order to suppress the parasitic NPN bipolar transistor from turning on, a p-buried layer underneath the source is necessary to reduce the base resistance for a higher holding and trigger voltage [23]. In this process, the p-type buried layer may be the reason that cause parasitic junction of nLDMOS doesn't show up during ESD case. The third device, which is named HVSCR+SH_P+HVPB is a simple structure to verify the conjectures.

The TLP results of three different HVSCR devices are shown in Fig.4.4. The simple HVSCR can successfully snapback and get a higher It_2 level. The trigger voltage increase when adding more highly doping layer. As the effective doping concentration increase, the parasitic bipolar junction becomes more difficultto turn on. The device with both SH_P and HVPB in the cathode cannot get into the snapback region.That is the main reason that causes the premature fail. So the It_2 level of the third device is the lowest one. The size of those SCR devices is 200μm for ESD performance cooperation.

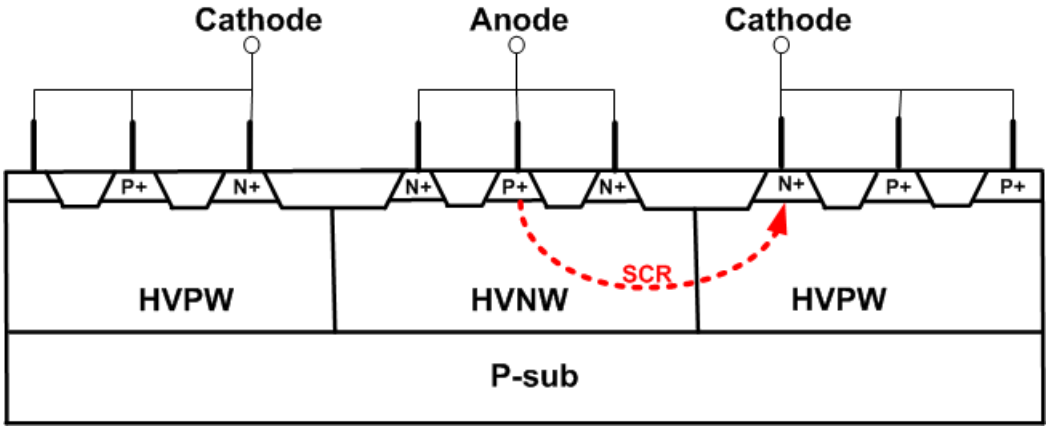


Fig. 4.1 The cross-sectional view ofsimple SCR structure which is named HVSCR.

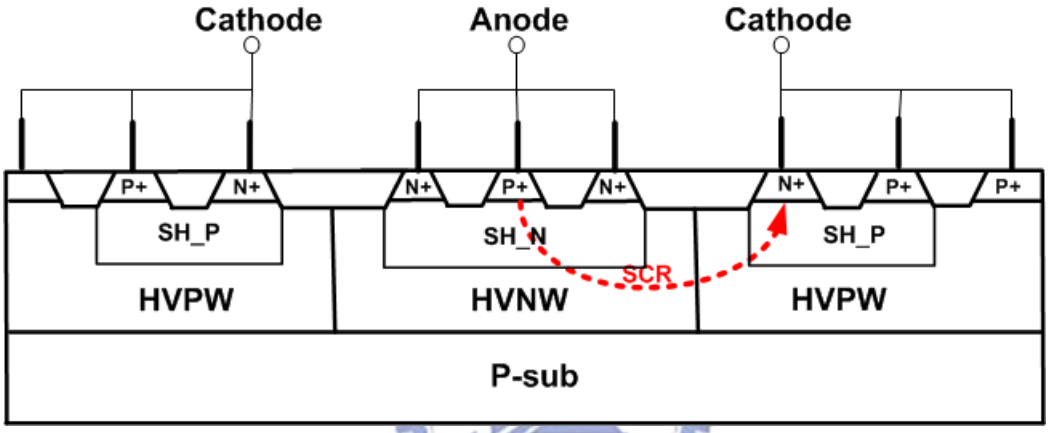


Fig. 4.2 The cross-sectional view ofsimple SCR with additional SH_N and SH_P layer structure (which is named HVSCR+SH_P).

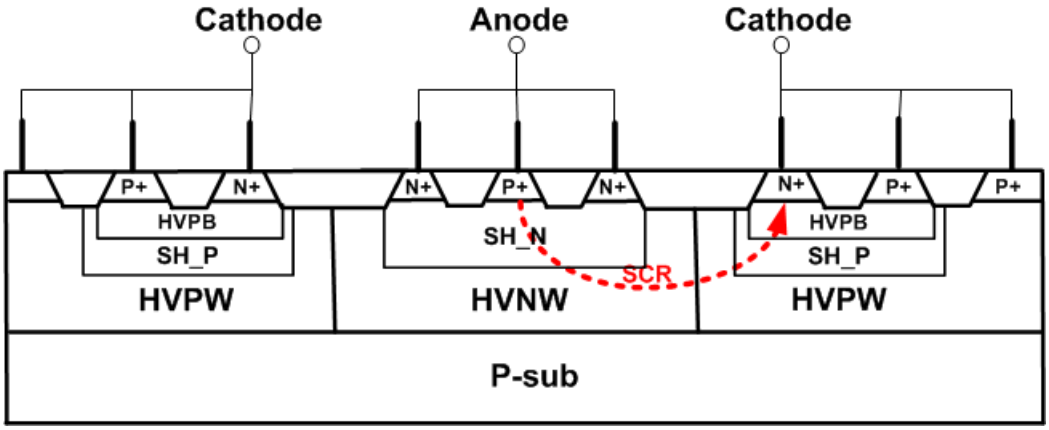


Fig. 4.3 The cross-sectional view of HVSCR+SH_P+HVPBdevice which is based on HVSCR+SH_P device with HVPB layer structure.

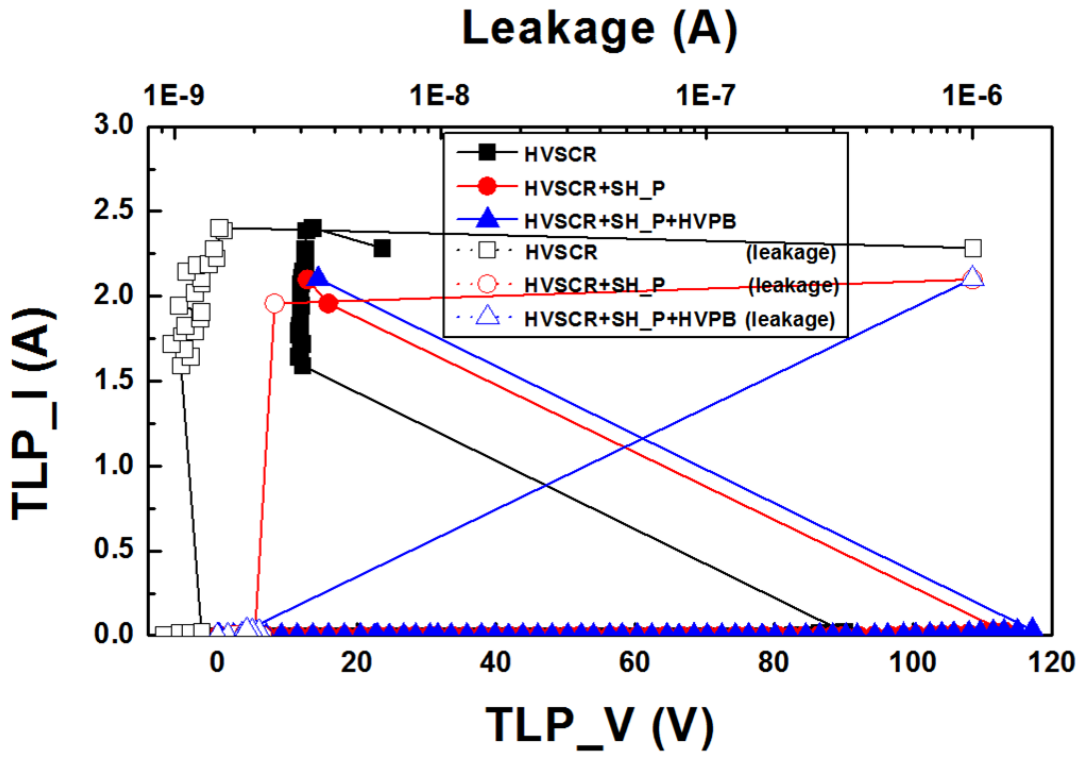


Fig. 4.4 The TLP results ofthree different HVSCR devices.

4.1.2Adding more implant in the anode side

Like the reason of drain-side engineering of nLDMOS, having some engineering the anode side of SCR is a kind of choices. Fig. 4.5 shows thecross-sectional view of reference HVSCR structure of anode side engineering (which is named HVSCR-A-pn-ref). HVSCR-A-pn-ref device uses the same layer of HVSCR in section 4.1.1 but with the different space from the p+ contact of anode to the edge of HVNW. As discussed in 4.1.1,the SCR path can appear during the ESD bombarded.One of the drawbacks of SCR structure is that the holding voltage is too low. The low holding voltage would let the device suffer from latchup issue. Increasing the holding voltage becomes the main issue of the SCR structure. The new proposed HVSCR structure, which is named HVSCR-A-pn, is shown in Fig. 4.6. The device has been added more n+ and p+ implants in anode. The dummy gate between

two p+ implantations is placed to reduce the total width. HVSCR-A-pn and HVSCR-A-pn-ref have the same parameter A, which is the space between N+ contacts in anode to HVNW edge.HVSCR-A-pn-ref structure is design to decrease the difference between the trigger voltage and the holding voltage.

The TLP results ofthese devices are shown in Fig.4.7. Both devices can successfully snapback. The holding voltage of HVSCR-A-pn is 10.2 V which is bigger than HVSCR-A-pn-ref (8.6 V). Both breakdown voltage and trigger voltage is the same. Even though the It_2level of HVSCR-A-pn is a little bit lower than that of HVSCR-A-pn-ref, but it is still large enough to pass the 8kV standards of HBM. Though adding the additional n+ and p+ implants can increase the holding voltage without change the trigger voltage.The holding voltage of HVSCR-A-pn is still not large enough to immune the latchup issue.

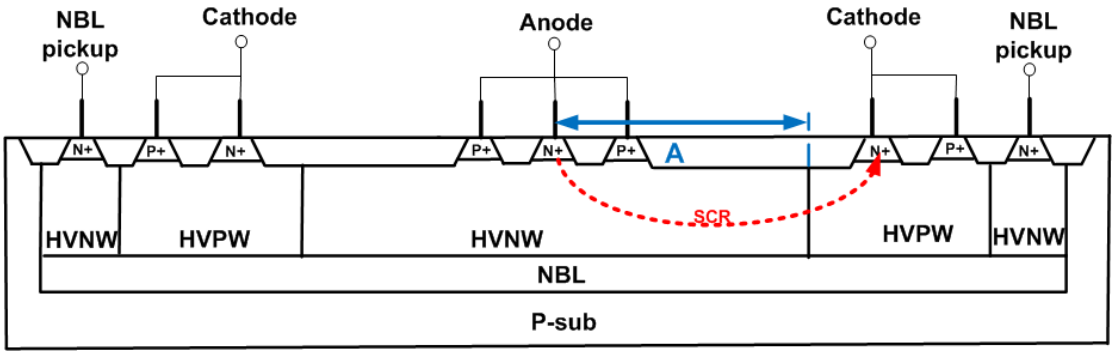


Fig. 4.5 The cross-sectional view ofreference HVSCR structure of anode side engineering (which is named HVSCR-A-pn-ref).

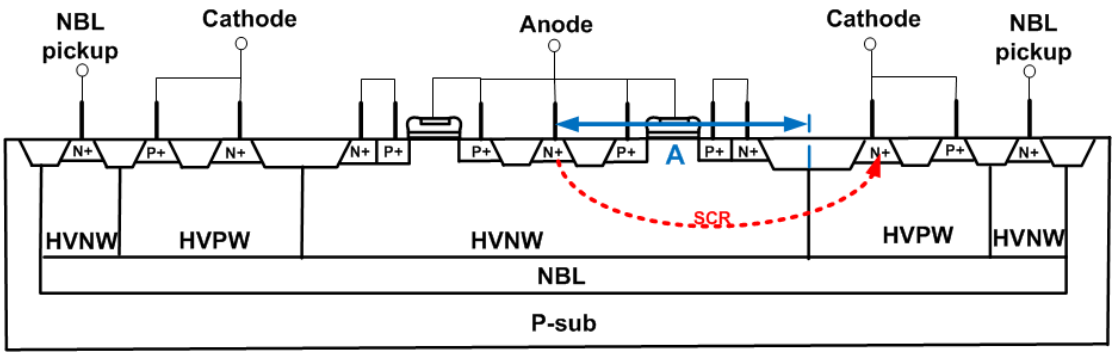


Fig. 4.6 The cross-sectional view of HVSCR structure of anode side engineering (which is named HVSCR-A-pn).

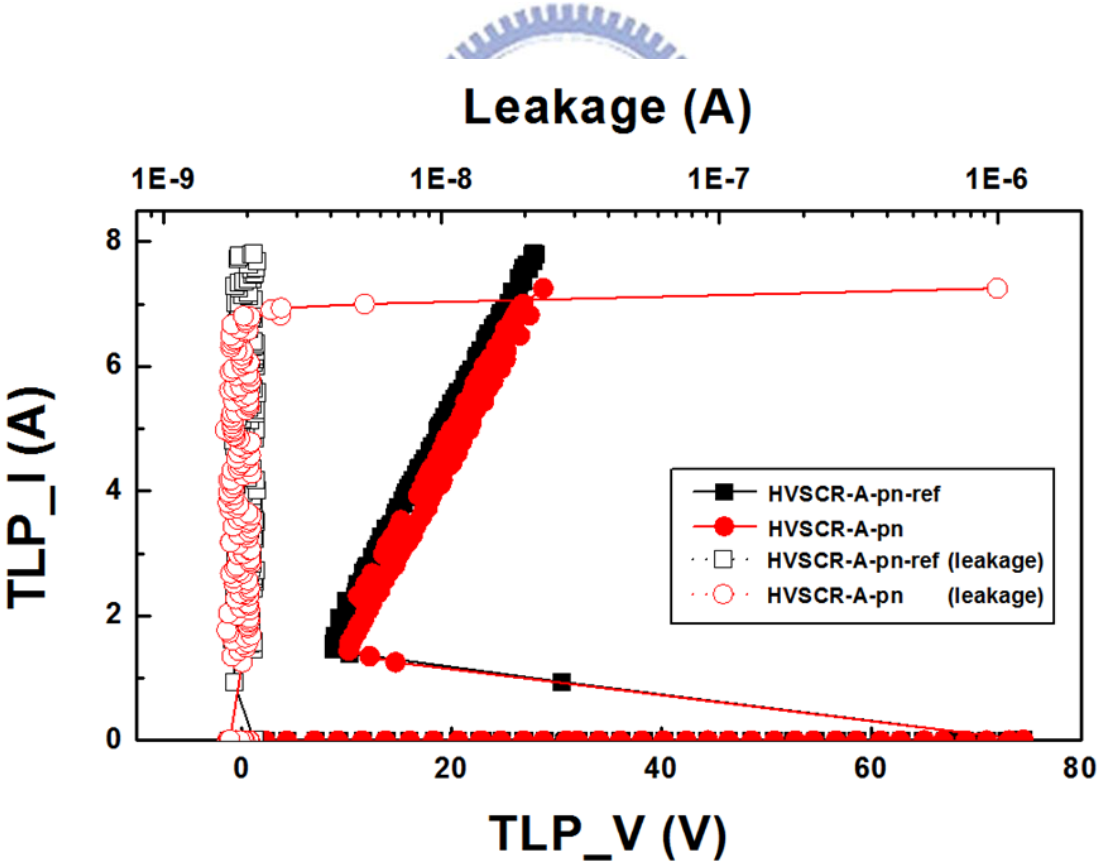


Fig. 4.7 The TLP results of HVSCR devices with additional implant layer in anode.

4.1.3Adding more implant in the cathode side

According to the measurement result of source side engineering of nLDMOS in section 3.3.2, adding more implants in the source side would increase the difficulty of parasitic BJT turn on and result in higher holding voltage. The similar structures have been studied in this section.Fig. 4.8 shows thecross-sectional view of reference HVSCR structure with larger parameter B when compares to simple HVSCR. The device named HVSCR-pnp-ref. The other structure is named HVSCR-pnp+pn in Fig. 4.9. HVSCR-pnp+pnhas been added more n+ and p+ implants in cathode. Like the structure of source side engineering of nLDMOS in section 3.3.2, there is a dummy gate between two n+ implantations to reduce the total width. To make sure the parasitic nMOS (N+ in cathode- HVPW-additional N+ node) always off, the dummy gate is connect to the cathode node. Those two devices in this section have the same parameter B, which is the space between N+ contacts in cathode to HVNW edge.

The new proposed structure HVSCR-pnp+pnhastheunexpected low breakdown voltage (41V),which is lower than the operation voltage (60V). So the following measurement about the leakage is bias at 30 V. **T**he TLP results ofthese devices are shown in Fig. 4.10. The holding voltage of HVSCR-pnp-ref is pretty low (6V). The holding voltage of HVSCR-pnp+pn is 13.4 V which is double of the HVSCR-pnp-ref. The It_2level is only 1.5A due to the high holding voltage.

The breakdown voltage is the major concern when using HVSCR-pnp+pn as an ESD protection device. There are two methods can solve the problem. One is to modify the layer order or the parameter to get an appropriate breakdown which at least higher than operation voltage. The other method is stacking. Stacking devices may let breakdown voltage, trigger voltage, and holding voltage increase. So the major design of HVSCR is how to get a lower the trigger voltage.

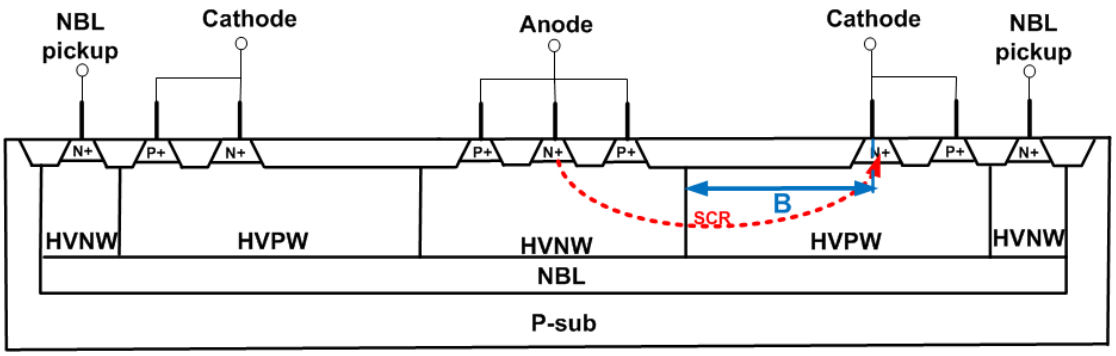


Fig. 4.8 The cross-sectional view of reference HVSCR structure of cathode side engineering (which is named HVSCR-pnp-ref).

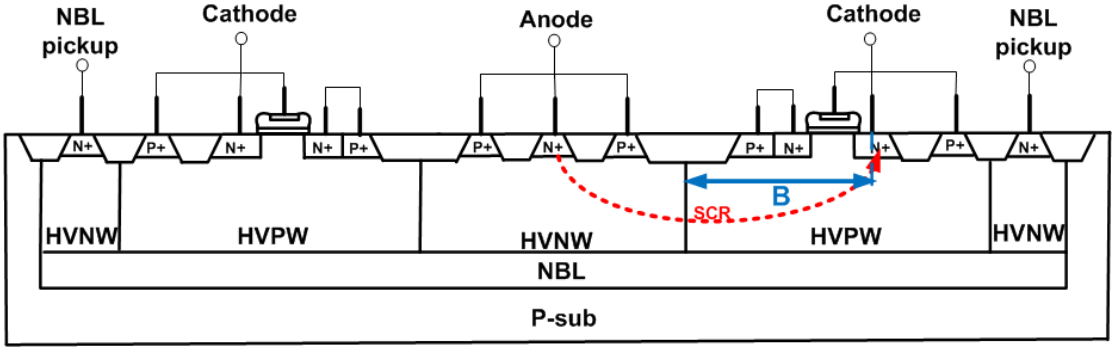


Fig. 4.9 The cross-sectional view of HVSCR structure of cathode side engineering (which is named HVSCR-pnp+pn).

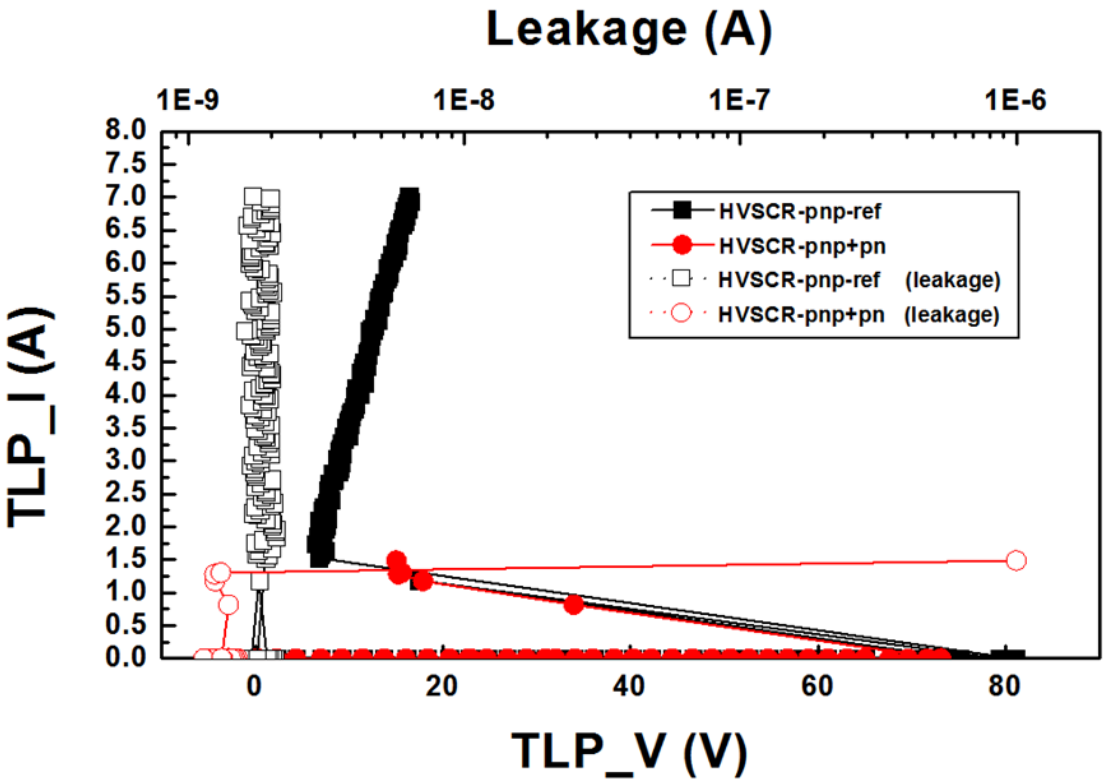


Fig. 4.10 The TLP results of HVSCR devices with additional implant layers in cathode.

4.2Device Modification of HVSCR

4.2.1 Layers modification of HVSCR

To correct the problem that breakdown of the device is lower than the operation voltage, the device in Fig 4.11 has the different arrangements of p+ and n+ implant layers in the anode side. As the reference [25], the different arrangement in the drain side of nLDMOScan have the different distribution of electrical field and current flows. And that mayaffectthose devices in the result of different trigger mechanism and breakdown voltage. Fig. 4.12 shows the schematics of two types of SCR. The difference between two types is the position of the p+ anode implant layer. The n+ implantation in type one is closer to gate region.In contrast, the p+ implantation is

more close to gate in type two.As illustrated in Fig. 4.13, the simulation shows the different current distribution of two types. The measurement results of the fabricated cells show in Fig. 4.14.Punch through effect may let the second type device decrease the breakdown voltage if the p+ implant layer in the anode locates too close to the interface between HVPW and HVNW. Especially in high voltage application, this effect may let the device cannot be used even in the normal operation condition. Hence, the arrangement of p+ and n+ implant layers in the HVSCR is as same as the first type. According to the TLP result, the breakdown voltage of this kind of HVSCR (~97V) is higher than the operation voltage (60V). The trigger voltage is also increased. Fortunately, the device can successful snapback before it get the permanent damage.

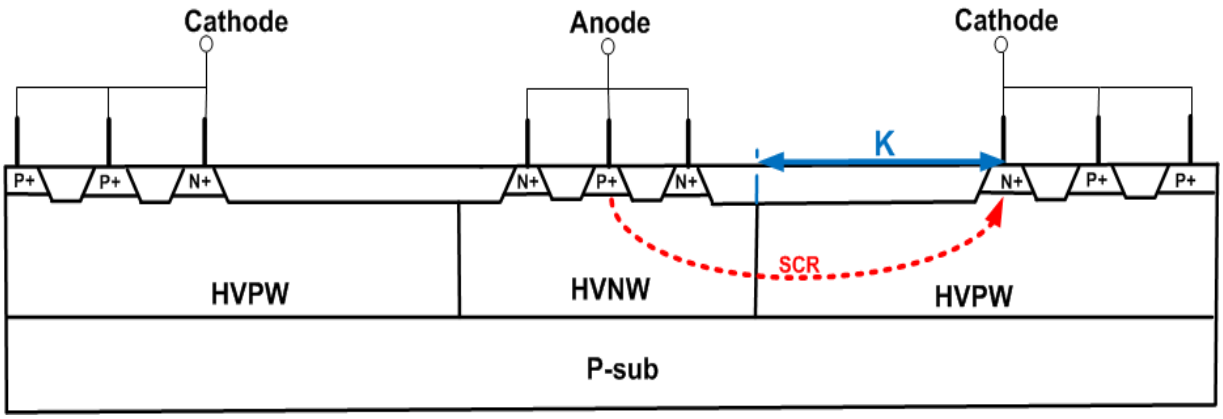


Fig. 4.11 The cross-sectional view ofdifferent arrangement HVSCR in cathode (which is named HVSCR-npn).

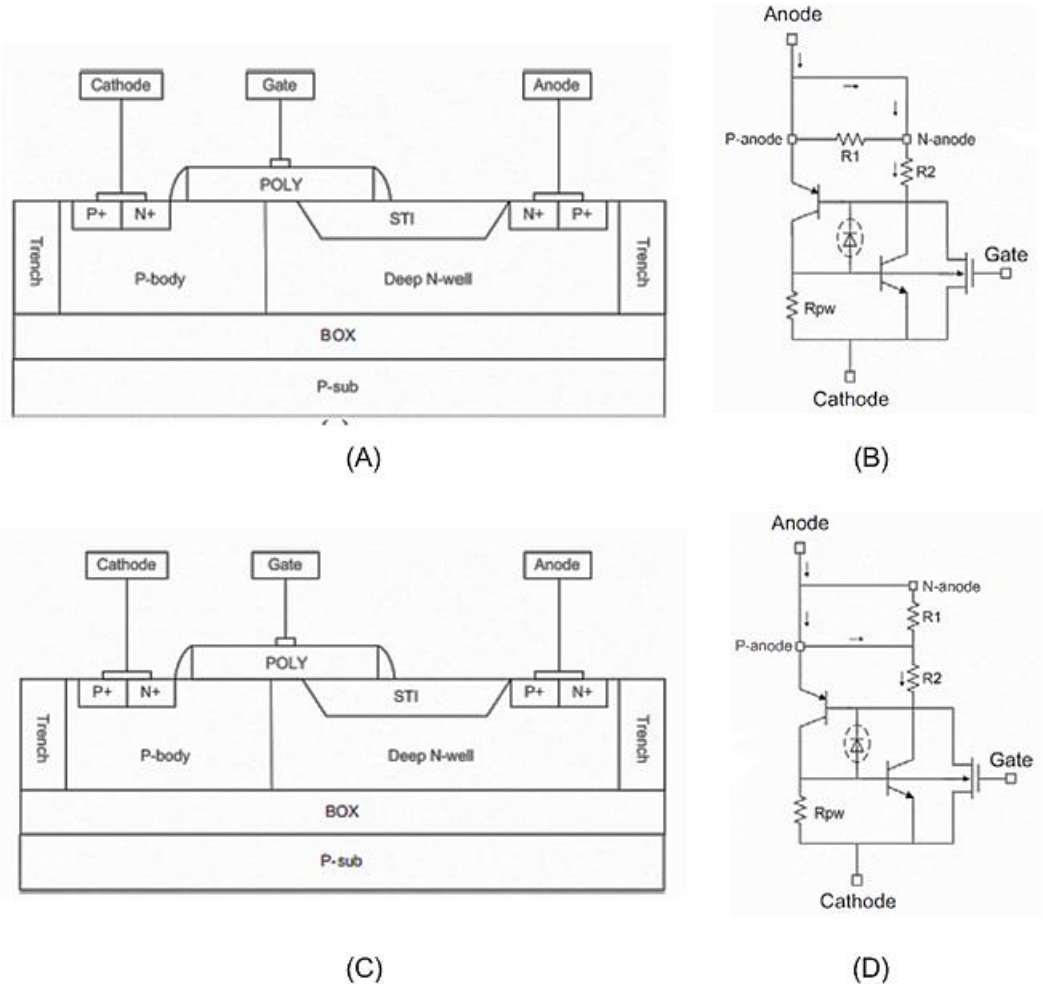
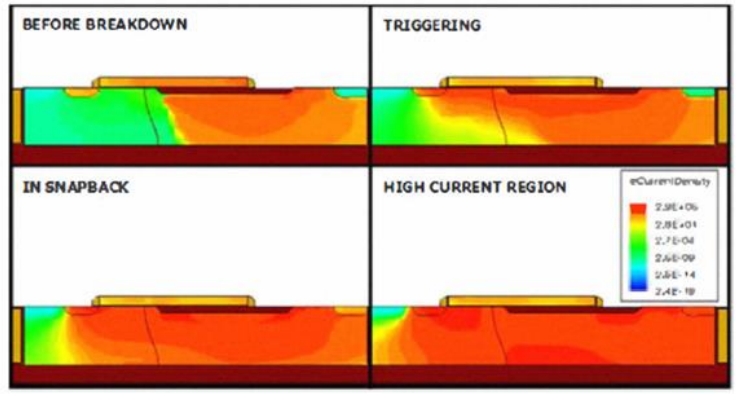
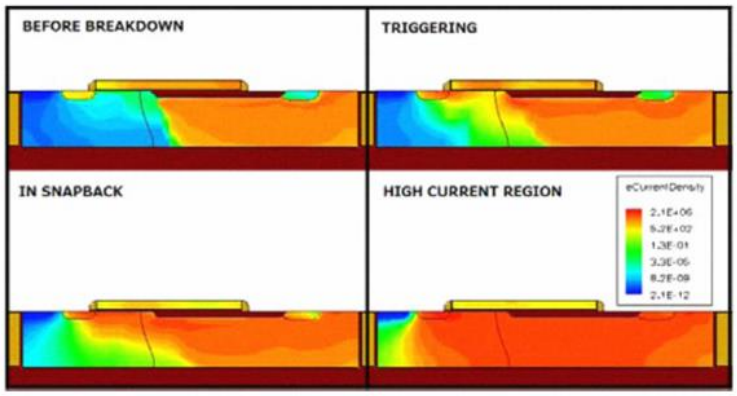


Fig. 4.12 The schematicsof two different types.(A) and (B) are the cross-sectional view and equivalent circuit of HVSCR of the type one, respectively. In contrast, (C) and (D) are the cross-sectional view and equivalent circuit of HVSCR of the type two. The length of PNPN SCR path is different of those two devices [25].



(A)



(B)

Fig. 4.13 The current distribution simulation of two different types[25].

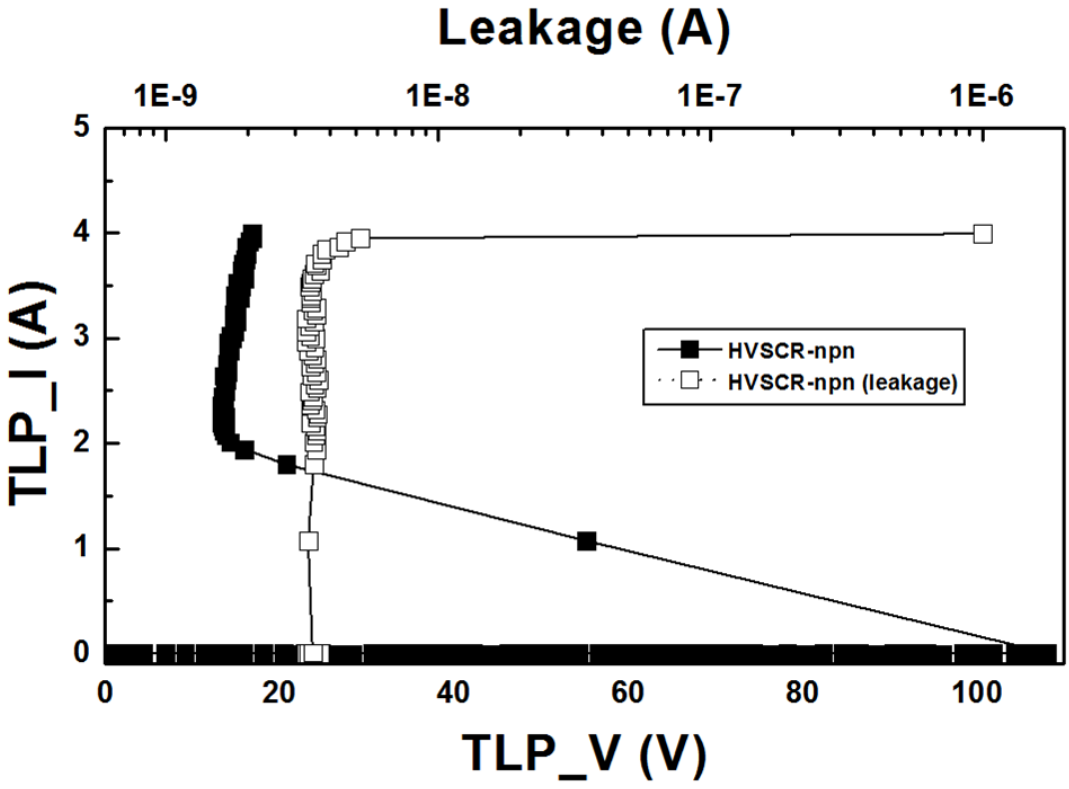


Fig. 4.14 The TLP results ofHVSCR-npn device.

4.2.2Layers modification of the SCR device with cathode-side engineering

Base on section 4.2.1, the holding voltage still too low to restrainlatchup. In order to cope with the low-holding voltage issue, adding additional p+ and n+ layers technique is going to be used in this section. As well as layer studied in section 4.1.1, adding the highly doping layer in HVSCR can increase the holding voltage. In the following, there are two groups of devices. Both groups haveadditional SH_N layer in anode side. The difference of two groups is in cathode. One group has both SH_N and SH_P in cathode. The other only has SH_P layer. Combining those two concepts, which have been mention as the methods of increasing holding voltage above, there are many different types of HVSCRs have been proposed as following.

Fig. 4.15 is the cross-sectional view of the HVSCR with more highly doping (SH_N and SH_P) layers when compare to HVSCR-npn in cathode.That device is named HVSCR-npn-SH_N because there is a SH_N implant layer in cathode. Adding additional n+ and p+ in the cathode side of HVSCR-npn-SH_N is called HVSCR-npn-SH_N+pn in the Fig.4.16. Then withadditional concept, which is calledSchottky emitter method[1],in HVSCR-npn-SH_N+pn deviceframethe device HVSCR-npn-SH_N+pnsho. This device is illustrated in Fig. 4.17. The ohmic contact is replaced by a shcottky junction, which is formed by SH_N in Fig. 4.17. Comparing those three devices' TLP results in Fig. 4.18, withadditional p+ and n+ (HVSCR-npn-SH_N+pn) can increase the holding voltage from 12 V to 26 V, which is double of the holding voltage of HVSCR-npn-SH_N device. But usingschottky emitter method and additional n+ and p+ implant layers together would let the device too difficult to be triggered. Measuring the fabricated device of HVSCR-npn-SH_N+pnsho can find out that device cannot snap back even bias even in pretty high voltage (160 V).

The group two has only SH_P layer in cathode. There are two kind of devices

have been compared of their ESD robustness in Fig. 4.19 and Fig. 4.20, respectively. The device in Fig. 4.19 is named HVSCR-npn-SH_P-D35 and the device in Fig. 4.20 is named HVSCR-npn-SH_P+pn-D35, which means HVSCR-npn-SH_P+pn-D35 device has additional p+ and n+ implant in the cathode side and the parameter D is 3.5μm to maintain the same area consumption of both two groups.

The TLP results of the group two is shown in Fig. 4.21. Both devices in group two has very high It2 level (> 7A). The holding voltage of HVSCR-npn-SH_N+pn is the highest in group two.

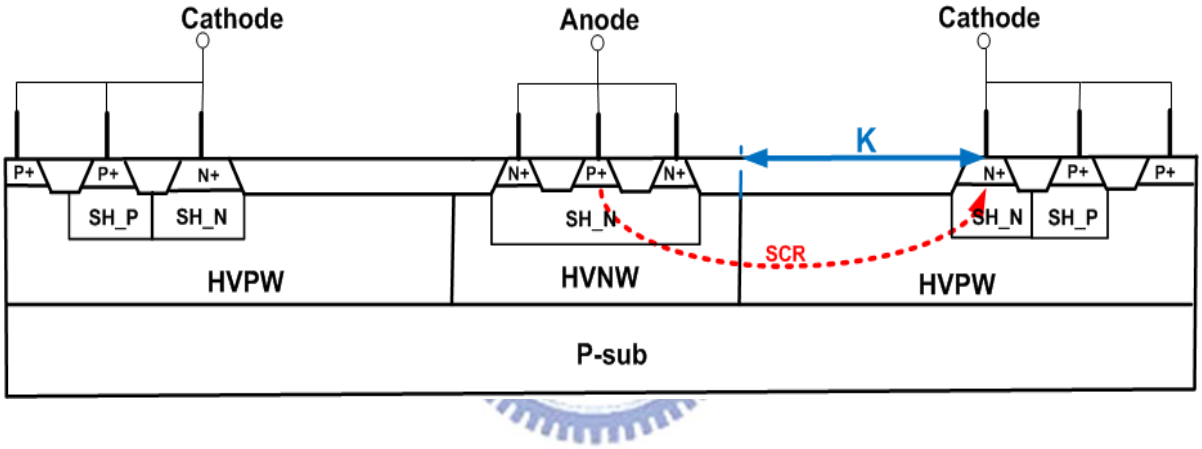


Fig. 4.15 The cross-sectional view of HVSCR-npn with additional SH_N and SH_P layer in both anode and cathode (which is named HVSCR-npn-SH_N).

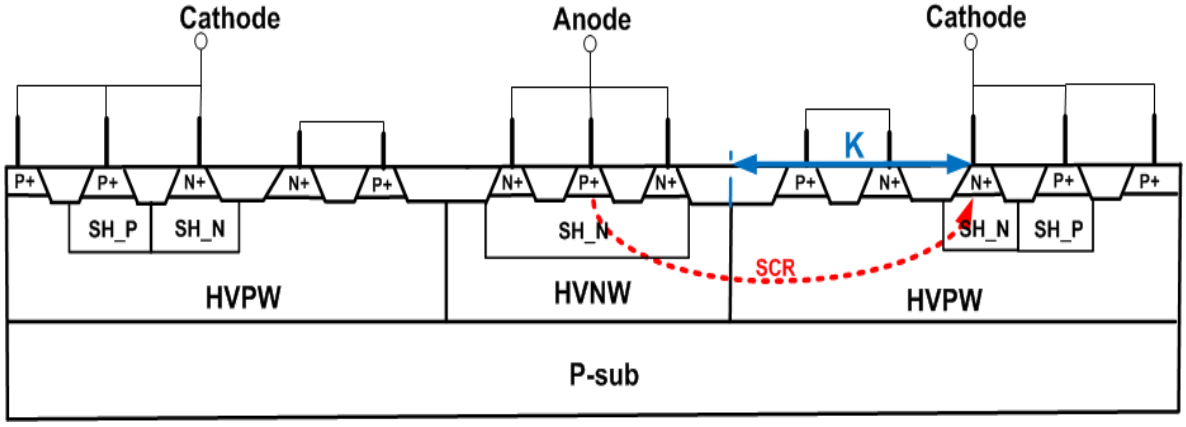


Fig. 4.16 The cross-sectional view of HVSCR-npn-SH_N+pn, which is HVSCR-npn-SH_N device with addional n+ and p+ in cathode.

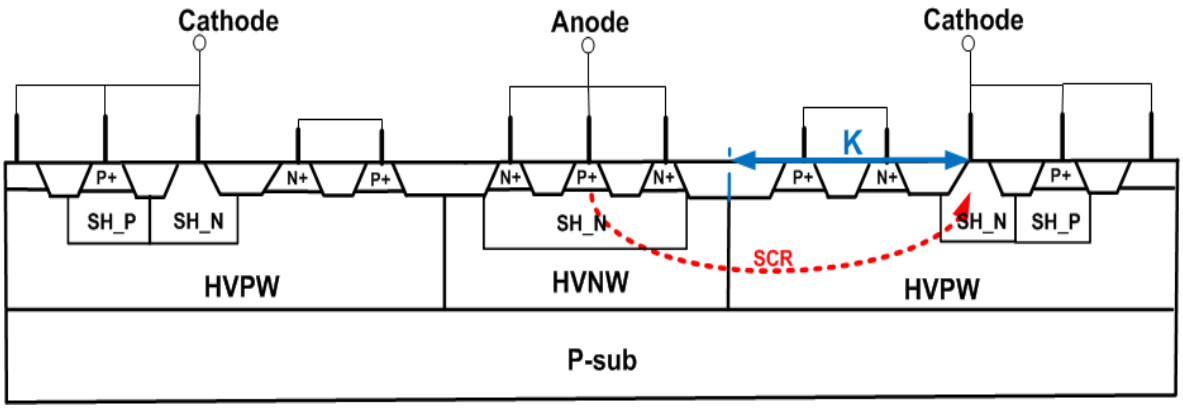


Fig. 4.17 The cross-sectional view of HVSCR-npn-SH_N+pnsho, which is addional n+ and p+ in cathode method and the Schottky emitter technique.

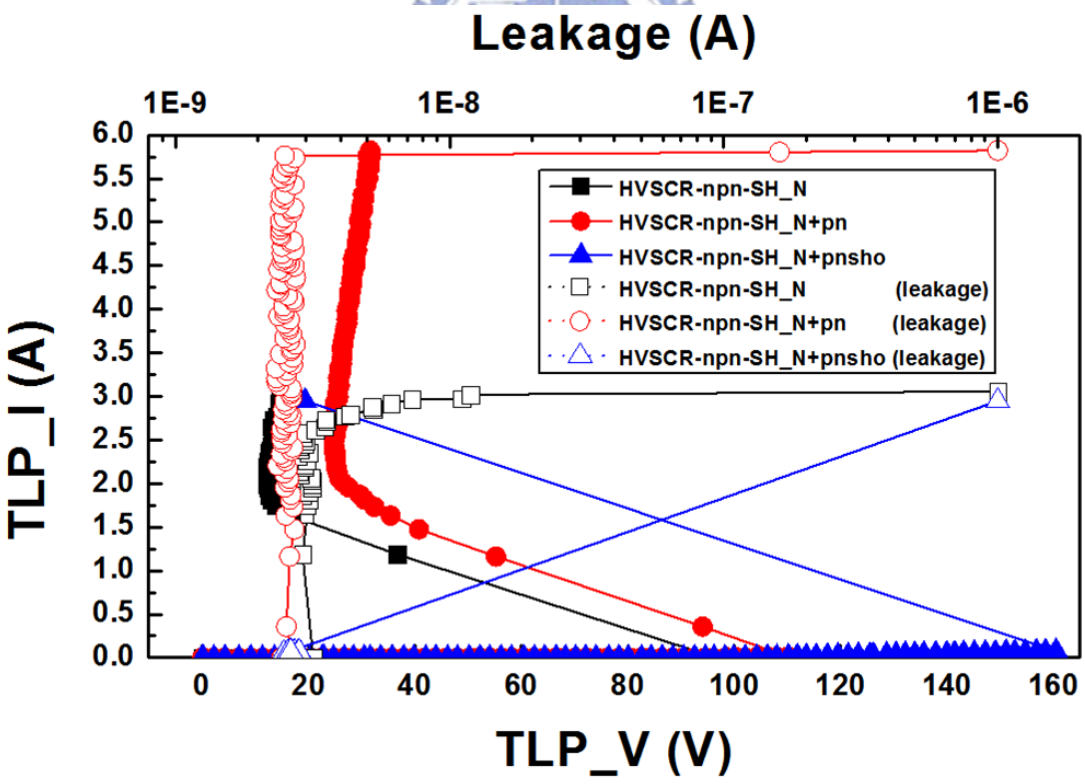


Fig. 4.18 The TLP results of three different types of HVSCR with SH_N and SH_P in the cathode region.

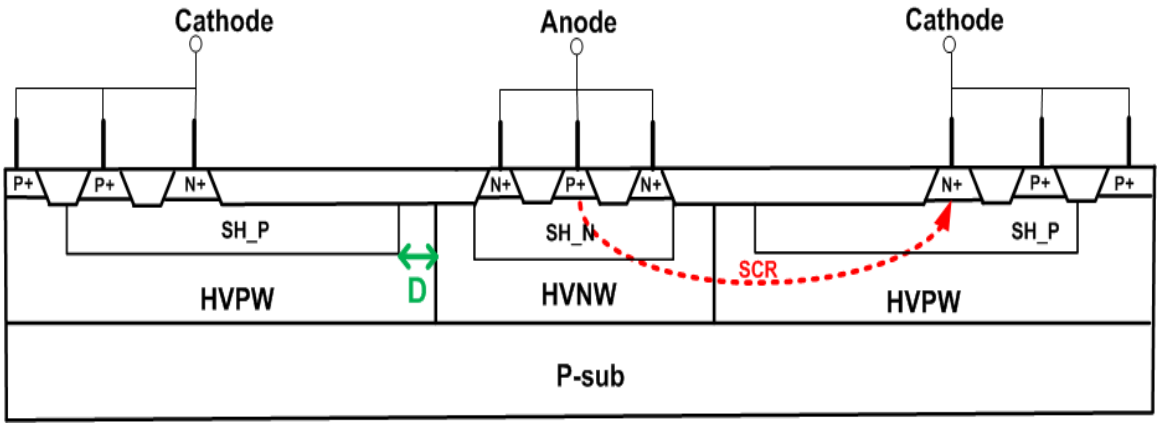


Fig. 4.19 The cross-sectional view of HVSCR-npn with only SH_P layer in cathode (which is named HVSCR-npn-SH_P-D35).

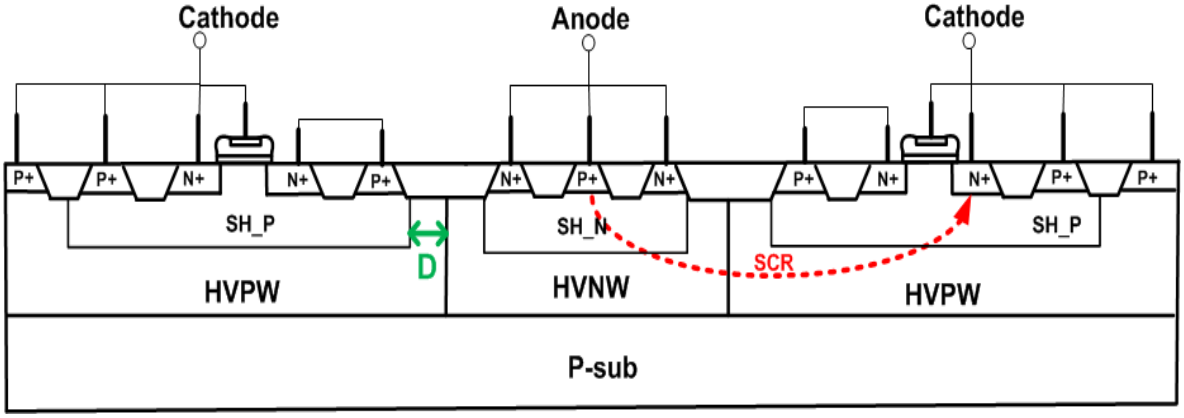


Fig. 4.20 The cross-sectional view of HVSCR-npn-SH_P+pn-D35, which is the HVSCR-npn-SH_P-D35 device with additional n+ and p+ implantation in cathode.

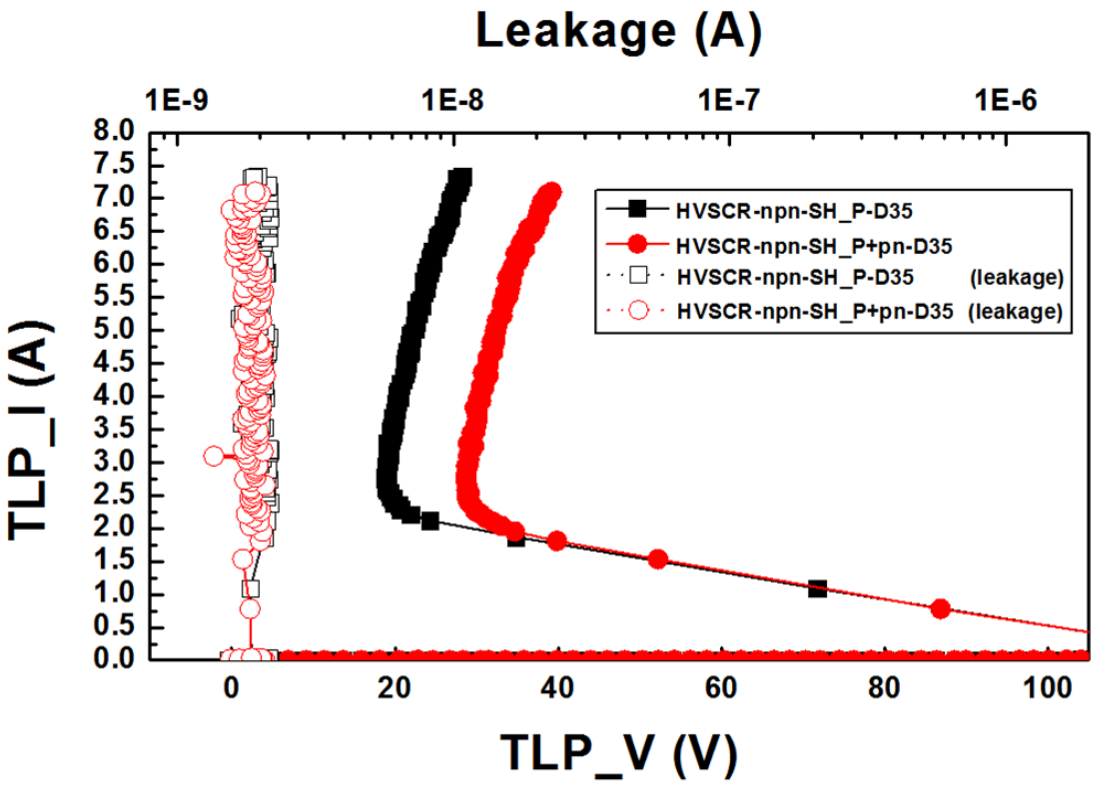


Fig. 4.21 The TLP resultsof those devices in group two, which only has SH_P layer in cathode region.

4.2.3Stretching the parameter of the SCR device

The parameter D in Fig. 4.19 and Fig. 4.20 can modulate the breakdown voltages, trigger voltages, and holding voltages of the device. The comparison of the device in Fig. 4.19 and Fig. 4.20 is shown in Fig.4.22. In Fig. 4.22, those devices have the minimum space of D which is the limit by technology file. Fig 4.23 shows the difference of three kinds of voltage between different parameter D.

Those three kinds of voltage would increase with the parameter D increase. But the slopes are different. The breakdown voltage increases more than the holding. So, stretching the parameter D is not a good way to prevent the latch up.

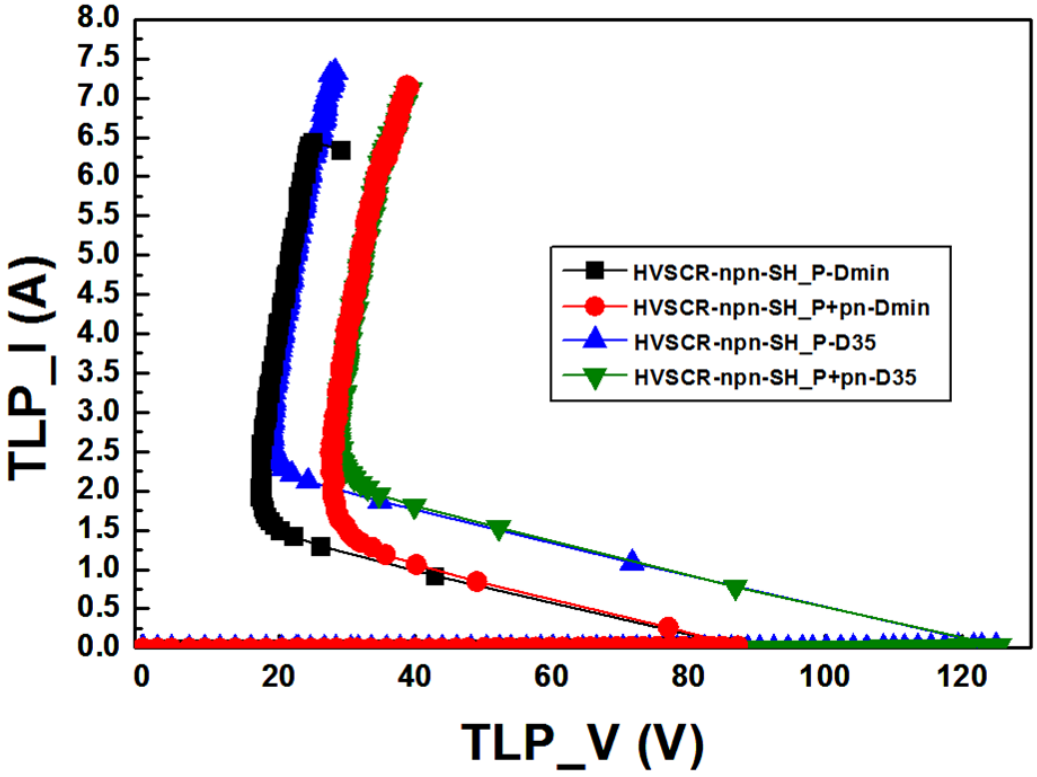


Fig. 4.22 The TLP results of two different devices in group two with different parameter D.

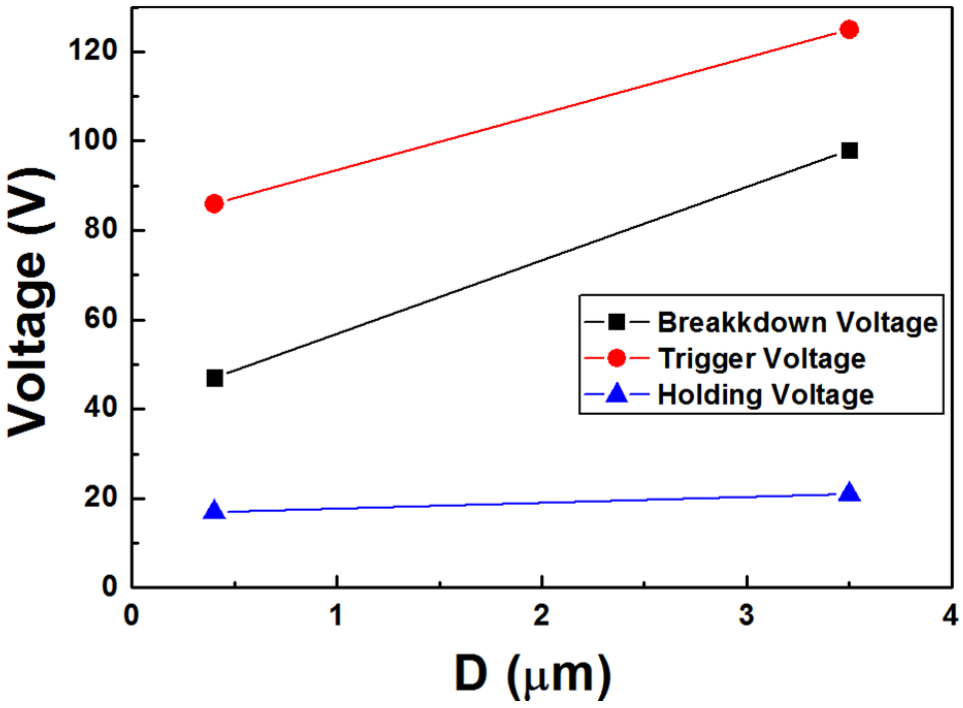


Fig. 4.23 The comparison between HVSCR-npn-SH_P-D35 and HVSCR-npn-SH_P-Dmin.

4.3The Proposed LVSCR Design in HV Process

Nowadays, in many high voltage applications, single processmay have many differentdevices which operate in different supply voltage. Since multiple voltage domain applications, ESD protection devices with tunable operation voltage are highly desirable. So, in the section, the LV ESD protection devices have been studied.

In LV device, silicon-controlled rectifier (SCR) device is known as anefficient device for electrostatic discharge protectionsince it can have the highest ESD robustness in the smallestlayout area. However, the main concern of SCR deviceused in CMOS ICs is the latchup issue. Some noises maymis-trigger the SCR device during normal circuit operations tocause the IC function failure.Three conventional methods have been presented to solvethe latchup problem in previous studies. The first method is toincrease the triggered current of SCR [31]. In addition, someadditional epitaxial or isolation layers were used to improvelatchup immunity of the SCR for ESD protection [32]. Thesecond method is to dynamically modulate the holding voltageof SCR. The idea of dynamic holding voltage is to adjust theholding voltage of SCR by changing the gate bias of theembedded nMOS and pMOS to avoid latchup issue [33]. Thethird method is to increase the SCR holding voltage [34], [35]. Ifthe holding voltage of SCR is higher than the normal supplyvoltage, it will be free from latchup issue. This method maydecrease the ESD robustness due to the higher heat generationduring ESD current discharging. In this section, a new design isproposed to increase the holding voltage of the SCR devicewithout decreasing its ESD robustness in a compact layoutarea.

4.3.1 Adding more implant in the cathode side

As illustrated in section 4.1.3, the same structures are used in LVSCR in high voltage process. Two SCR structures are compared in this work, which arelabeled as LVSCR-pnp and the LVSCR-pnp+pn inFig. 4.24, respectively.

A transmission-line-pulsing (TLP) system is used to measurethe breakdown voltage, holding voltage, and the maximumcurrent-handling ability (the second breakdown current, It2) ofthe fabricated devices. The failure criterion is defined as theleakage current over 1 μA under the 5V biascondition. The TLP measurement results of the fabricated SCR devicesare shown in Fig. 4.25. The breakdown voltage of LVSCR-pnpis ~22V and the holding voltage is~3V. This device may suffer fromlatchup issue by noise triggering inthe normal operation condition due to the supply voltage (5V) is larger than 3V. Comparing tothe measurement result of LVSCR-pnp+pn,the holding voltage is increased to~7.7V, while the breakdown voltage unchanged. Besides, themaximum current-handling ability (It_2) of the LVSCR-pnp+pn is not degraded, which is still as high as ~7.5 A.

To make sure that the ESD robustness of the new proposedSCR is not degrade, the human-body-mode (HBM) andmachine-mode (MM) ESD tests have been performed to thefabricated devices by the ESD tester. The failure criterion isdefined with 30% of breakdown voltage shift after ESD stress.The conventional SCR can pass 8-kV HBM and 800-V MMESD tests, which are the voltage limitation of a given ESDtester. The new proposed SCR can also pass the 8-kV HBM and800-V MM ESD tests. This result confirms that the newproposed SCR does not degrade the ESD robustness.

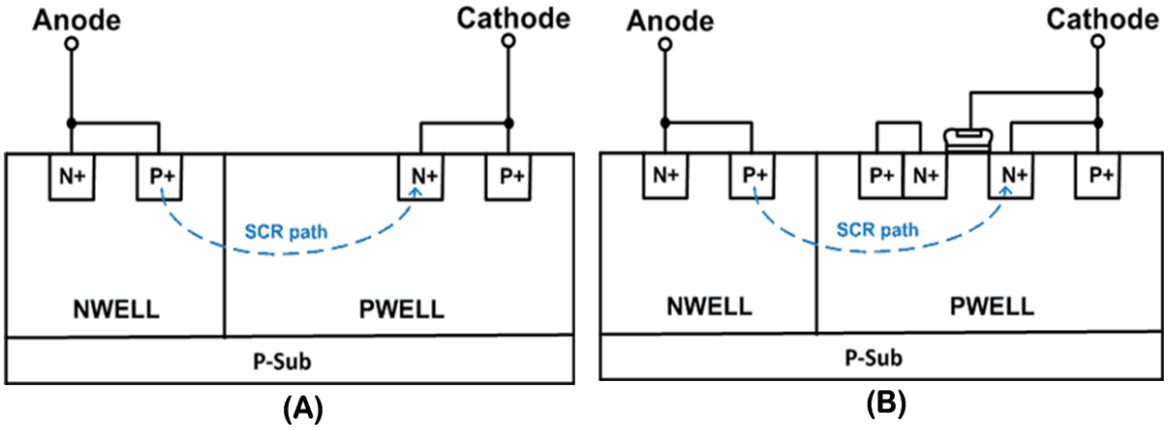


Fig. 4.24 The cross-sectional view of (A) LVSCR-pnp and (B)LVSCR-pnp+pn.

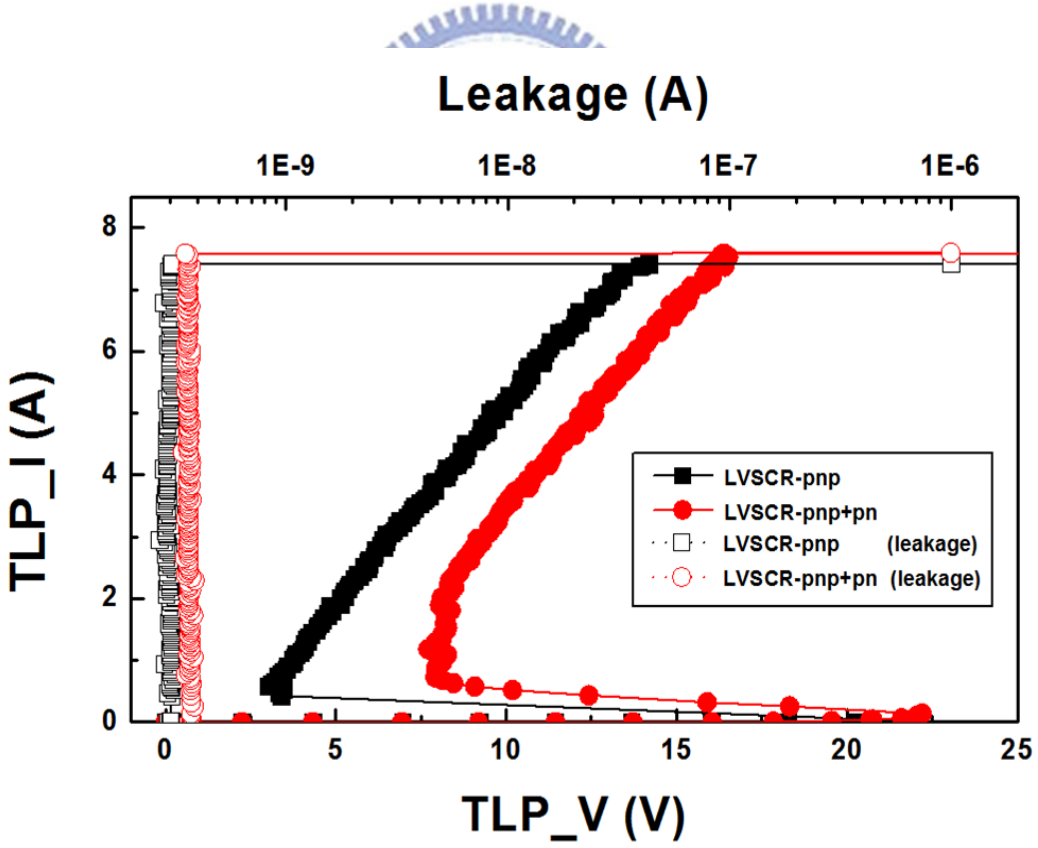


Fig. 4.25 The TLP resultsof LVSCR-pnp andLVSCR-pnp+pn.

4.3.2 Other Modification of LVSCR

In this section, the p+ and n+ implantations is going to rearrangement in the anode side. The two different devices (with and without the additional n+ and p+ implants in the cathode side) are shown in Fig. 4.26 and Fig. 4.27.If the device in Fig.4.27 is drawn in minimum rule (named LVSCR-npn+pn-H6), which means the parameter G is 0.5μm, then the relative length of parameter H is equal to 6.5μm. The reference device without additional p+ and n+ in the cathode is named LVSCR-npn-H6, which has the same parameter H as the device LVSCR-npn+pn-H6. The TLP result of these two devices has been shown in Fig. 4.28. I-V curve of LVSCR-npn-H6 is weird and it has a premature ESD failure.

The device in Fig.4.27 is drawn in the same rule of HVSCR (named LVSCR-npn+pn-H10), which means the parameter G is 3.5μm and the relative length of parameter H is 10μm. The reference device without additional p+ and n+ in the cathode is named LVSCR-npn-H10, which has the same parameter H as the device VSCR-npn+pn-H10. The TLP result of these two devices which have a large parameter H has been shown in Fig. 4.29. I-V curves of both devices become normal. Comparing the device which has highest It_2 level in different parameter H in Fig. 4.30, the smaller H with additional p+ and n+ have lower trigger and holding voltage. Stretching the parameter G of LVSCR to 3.5μm can get the higher holding voltage which has weak snapback characteristic.

The relationship between the three kinds of voltage (such as breakdown voltage, trigger voltage, and holding voltage) and the parameter H is shown in Fig 4.31. Trigger voltage and holding voltage would increase with the parameter H increases. Butthe breakdown voltage remains the same. This result is quite different to those in HVSCR.

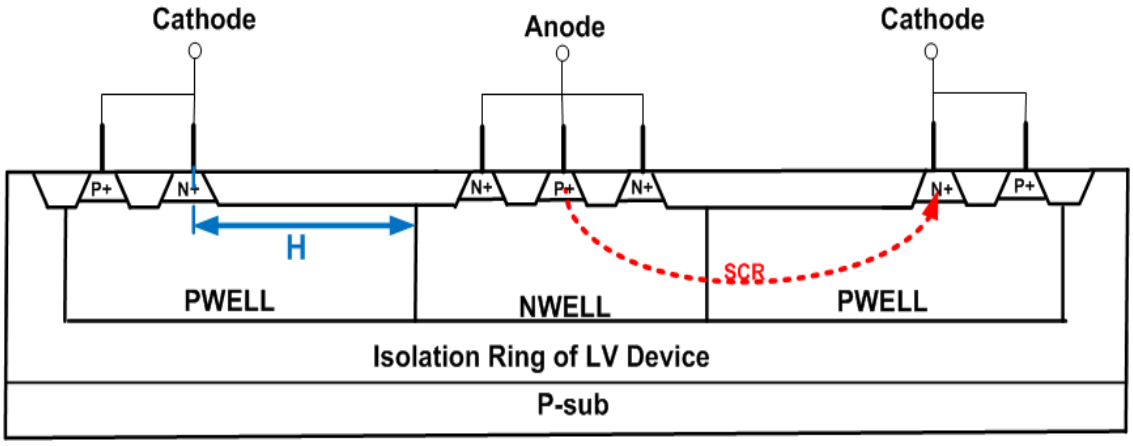


Fig. 4.26 The cross-sectional view of LVSCR-npn. There are two different parameter H is proposed which name as LVSCR-npn-H6 and LVSCR-npn-H10, respectively.

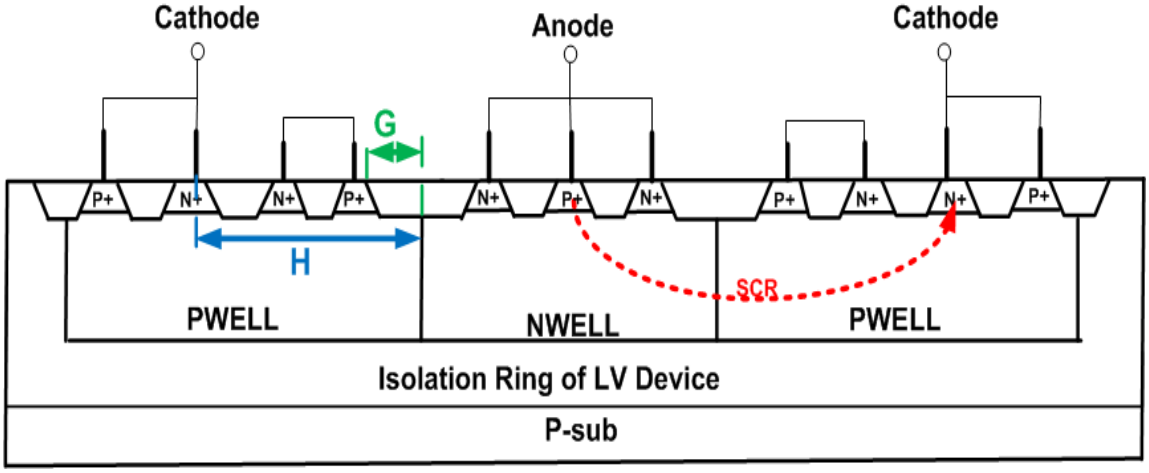


Fig. 4.27 The cross-sectional view of LVSCR-npn+pn. There are two different parameter H is proposed which name as LVSCR-npn+pn-H6 and LVSCR-npn+pn-H10, respectively.

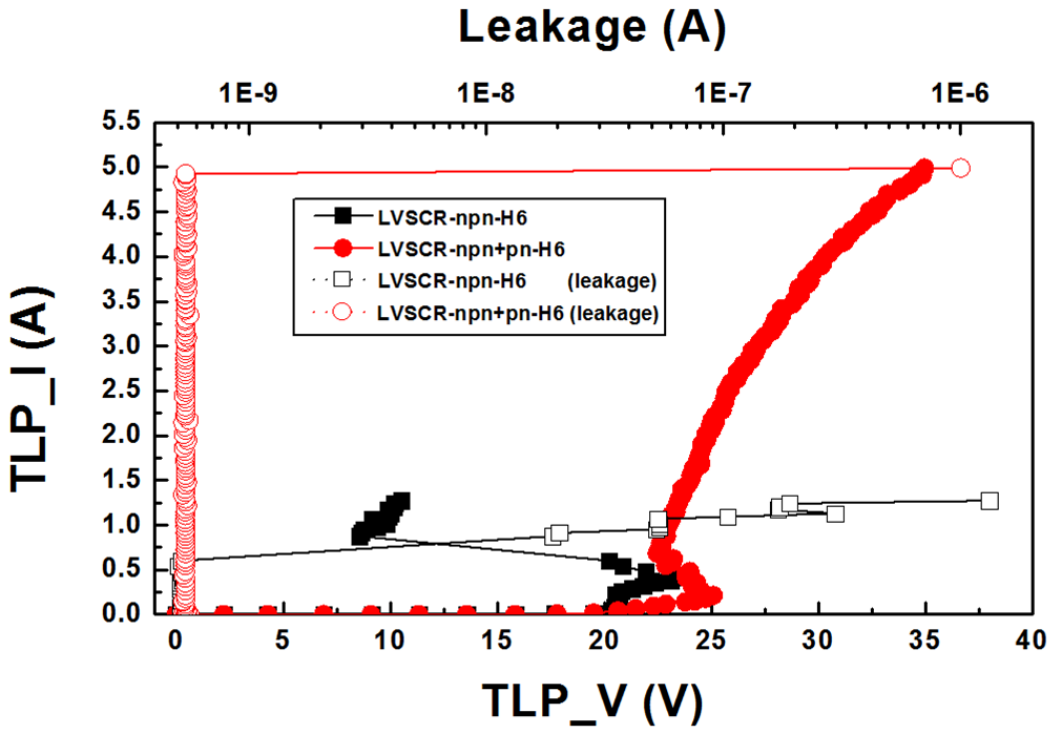


Fig. 4.28 The TLP resultsof two different structures with same parameter H. (H is equal to 6.5μm)

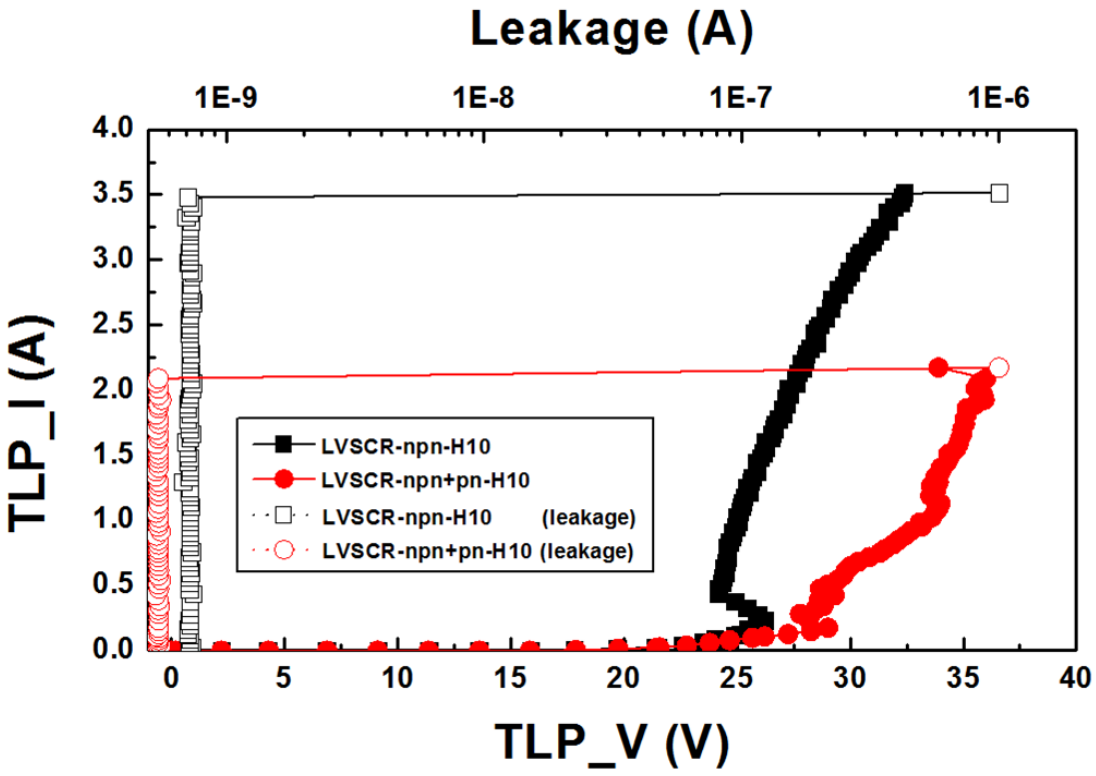


Fig. 4.29 The TLP resultsof two different structures with same parameter H. (H is equal to 10μm).

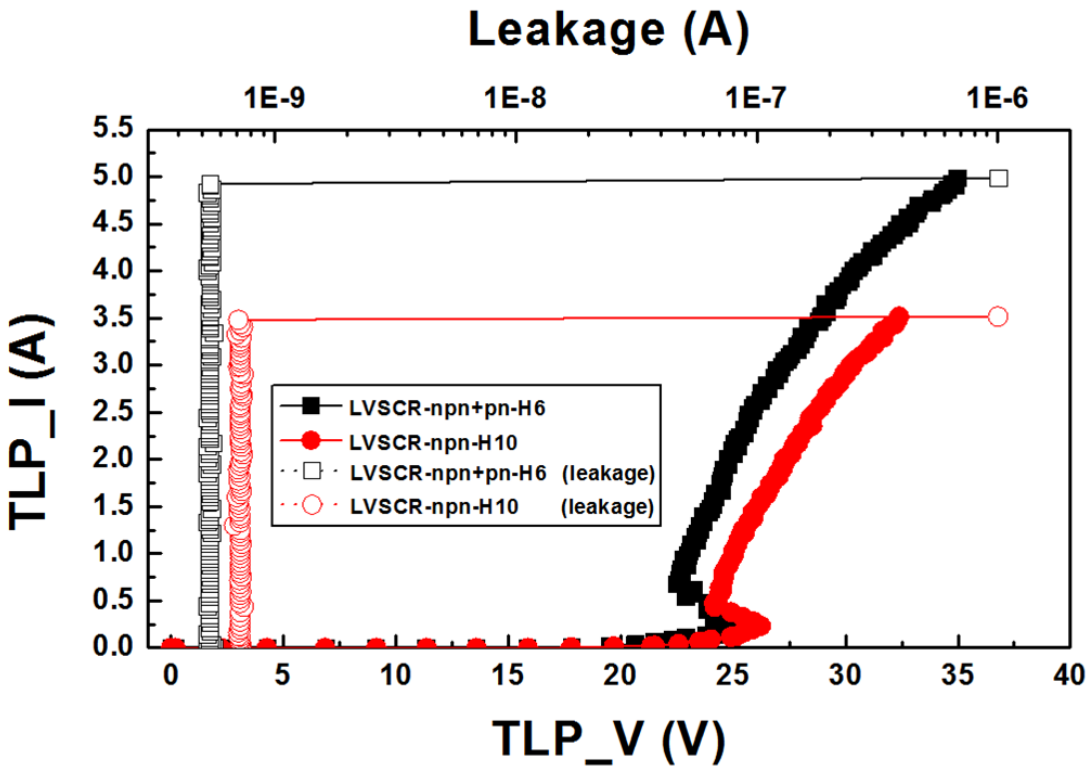


Fig. 4.30 The comparison of two different devices which has the highest It_2 level.

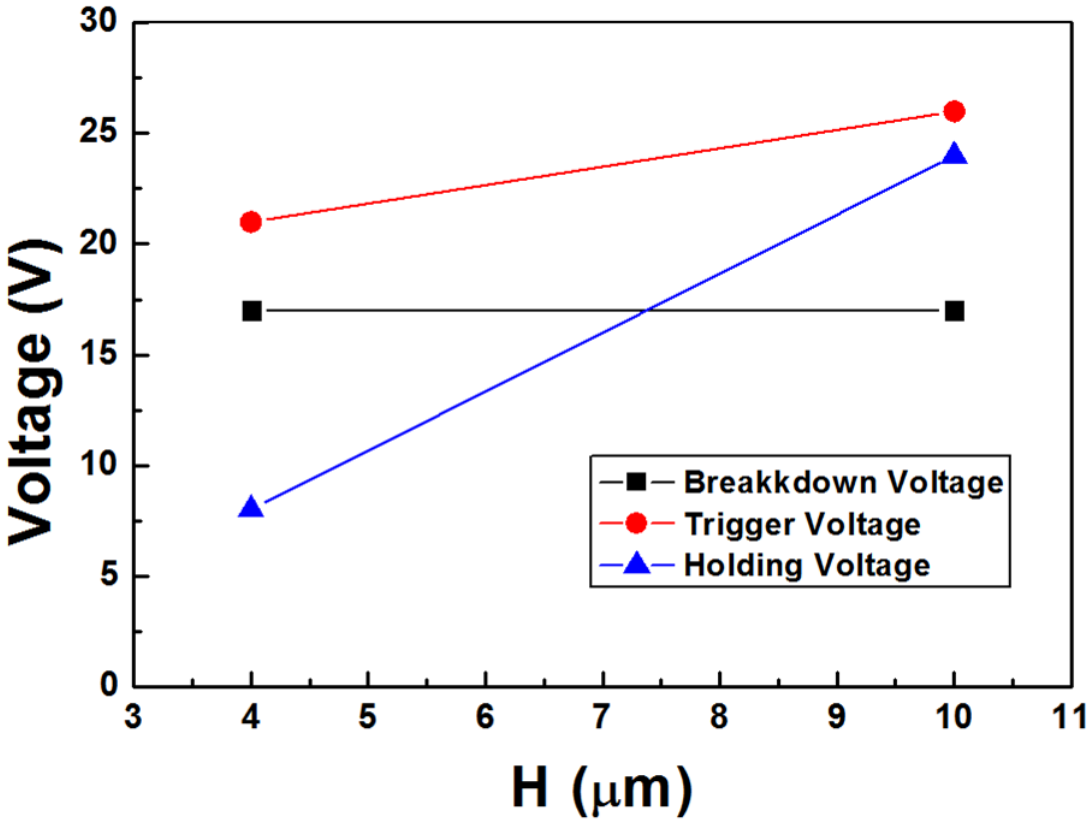


Fig. 4.31 The comparison between LVSCR-npn-H6 andLVSCR-npn-H10.

4.4 Discussion and Summary

4.4.1 Discussion

There are three different concepts of increasing the holding have been used in this chapter. The first idea is to modulate the equivalent doping concentration. Adding the SH_P layer would let the SCR difficult to turn on. Moreover, the HVSCR with the highly doping layer SH_P and HVPB layer would not get in to the snapback region before the device fail. This structure is similar to nLDMOS in 60V process. So conjecture about that HVPB layer causes the device premature failed is reasonable.

The second concept is about adding additional n+ and p+ implant layer in cathode. That additional parasitic BJT weakens the positive feedback of SCR. Take the LVSCR for example.The equivalent circuit of the conventional SCR is shown in Fig. 4.32 with the parasitic BJTs and resistors. During ESD stress, the NPN BJT (Q_n) may turn on first, and then it will help the PNP BJT (Q_p) to be turned on. The positive feedback of those two BJTs in SCR [38] is the reason why SCR can have such low holding voltage. To improve latchup immunity, the new structure of SCR with additional p+ and n+ layer in cathode is shown in Fig. 4.33. To increase the holding voltage of SCR, one more parasitic BJT (Q_n') is inserted into the device structure, which is shown in Fig. 4.33(a). The equivalent circuit of the SCR with additional p+ and n+ layer is shown in Fig. 4.33(b). During the turn-on operation of the SCR, the NPN BJT (Q_n) and the additional parasitic BJT (Q_n') turn on at the same time. The additional BJT (Q_n') clamps the voltage between base and emitter of the NPN (Q_n), which makes the positive feedback of BJTs weaken. That is, the additional BJT (Q_n') will break the positive feedback of the NPN and PNP BJTs. As a result, the holding voltage of this new proposed SCR will be higher than that of the conventional SCR. Therefore, the new proposed SCR may be free from latchup problem. This method is

fully process-compatible to the commercial CMOS processes without additional mask or process step in the chip fabrication. The same idea can be used in anode side in high voltage process. The detail results of these devices have been shown in Table 4.1. The holding voltage of the device with additional layer in anode is not increase that much than those in cathode.

Furthermore, there are two kind of implant layers arrangement of SCR in anode. One is the n+ implant layer near the interface of N-type and P-type well (which is symbolized by npn in device name). The other is the p+ implant layer near the interface of N-type and P-type well (which is symbolized by pnp in device name). The strength of the positive feedback, which is related to the space of the parasitic PNPN, determines the holding voltage. Hence, the arrangement would change the trigger and holding voltage due to the different distribution and turn on mechanism. No matter LVSCR or HVSCR, the holding voltage of those devices which are classified in pnp group has lower holding voltage than those in npn group. In LV device, the device in each group almost has the same trigger voltage. The trigger voltage of those devices in npn groups would increase if the device has additional p+ and n+ layers.

In HV device,which lists in Table 4.2, the trigger voltage of pnp group (device HVSCR-pnp-ref and HVSCR-pnp-pn) is lower than those in npn group (device HVSCR-npn). The worst thing is that the breakdown voltage of HVSCR-pnp-pn is lower than operation voltage (60V). If the p+ implant layer is the closer layer to the interface of HVPW and HVNW in both anode and cathode, this breakdown voltage lowering phenomenon would happen. All of the test devices mentioned in this stage are occupied the same layout area. To avoid the breakdown voltage lowering constraint, the following discussions are all based on the npn type HVSCR.

The third notion is changing the space between SH_P to HVNW edge in HV

device or the space between p+ implantation to Nwell edge in LV device. The comparison of space different in HV device is shown in Table 4.3. The device HVSCR-npn-SH_P-D35 has the larger parameter D than HVSCR-npn-SH_P-Dmin.As a result, all of the breakdown voltage, trigger voltage, and holding voltage of HVSCR-npn-SH_P-D35 is higher than those in HVSCR-npn-SH_P-Dmin. Combining with the second concept, which the adding additional p+ and n+ method, the holding voltage of the device with large D (HVSCR-npn-SH_P+pn-D35) increases from 21V to 28V and the holding voltage of the device with small D (HVSCR-npn-SH_P+pn-Dmin) raises from 17V to 28V. That is, adding additional n+ and p+ layers is more powerful in the small D case. Without stretching the device size, using the second concept can increase holding voltage even higher than the holding with large D. With additional p+ and n+ implantation in cathode, the holding voltage restricts to 28V, no matter what parameter D is. The comparison of different devices in LVSCR is shown in Table 4.4. In LV case, the breakdown voltage dominates by the doping concentrations of P-type and N-type well and less relates to the parameter H or G. The difference between with and without additional p+ and n+ implant layers in cathode is larger than those in the small parameter H (small H case increasing from 8V to 22V and large H case increasing from 24V to 27V). But unlike the results in HV process, both trigger voltage and holding voltage increase when adding more implantations in cathode. Those SCR devices have been fabricated in a 0.25-μm 60-V process. The total widths of all test SCR devices are drawn as 200μm for performance comparison.

According to the experimental results, the structure that namedLVSCR-pnp+pn has latchup immunity. For insurance, transient-induced-latchup (TLU) test system is used to simulate the latchup condition and qualify for the latchup immunity. TLU test is to simulate the noise condition under the normal operation. In normal condition,

transient overshoots on power-supply voltage can take place because of the noise coupling under system or environment disturbance. Those overshoots may let SCR be mis-triggered. The TLU setup is shown in Fig. 4.34 [38], where the MM ESD source is used to generate the transient noise into the power supply of device under test. Therefore, the parasitic BJTs in SCR may be mis-triggered by such transient noise. If it is affected by the latchup issue, the voltage waveform monitored in the oscilloscope will be clamped down to its holding voltage after transient noise triggering. The test results of the LVSCR-pnp and LVSCR-pnp+pn device are shown in Fig. 4.35 and Fig.4.36. In Fig. 4.35, after transient noise triggering with the initial V_{charge} of only 50V, the voltage across LVSCR-pnp is clamped down to ~2 V. On the contrary, the voltage across LVSCR-pnp is still kept at 5V, as shown in Fig. 4.36, even if the V_{charge} is up to 800 V during the TLU test. This result has been proved that the LVSCR-pnpwhich is a high latchup-immune device for 5-V circuit applications.

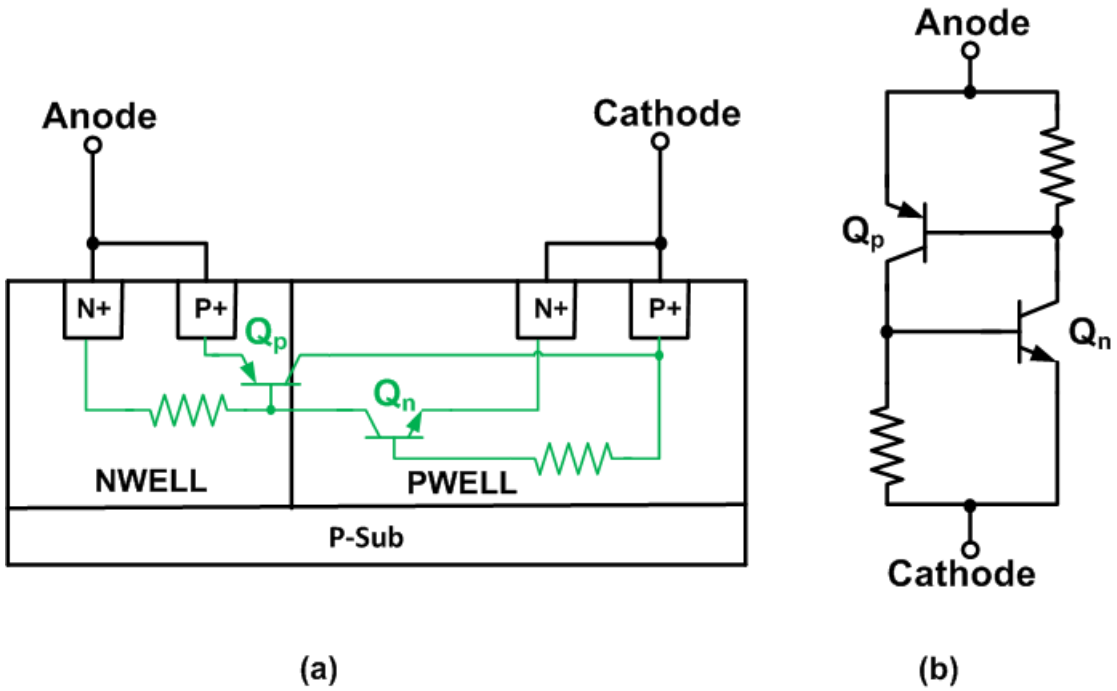


Fig. 4.32 (A) Cross-sectional view and (B)the equivalent circuit of LVSCR-pnp.

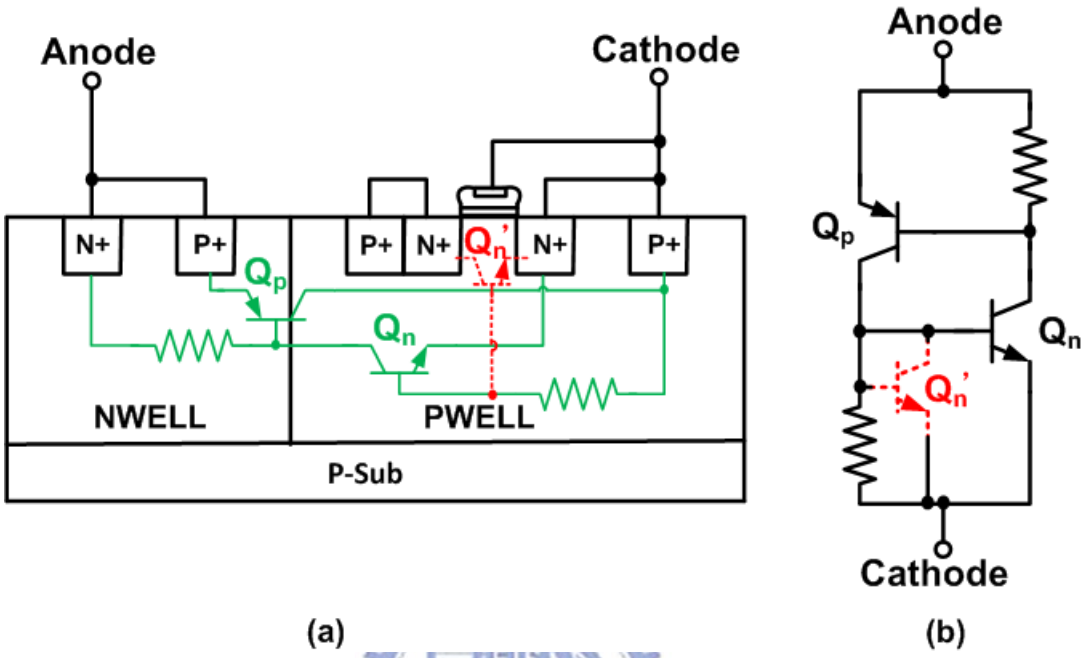


Fig. 4.33 (A) Cross-sectional view and (B) the equivalent circuit of LVSCR-pnp+pn.

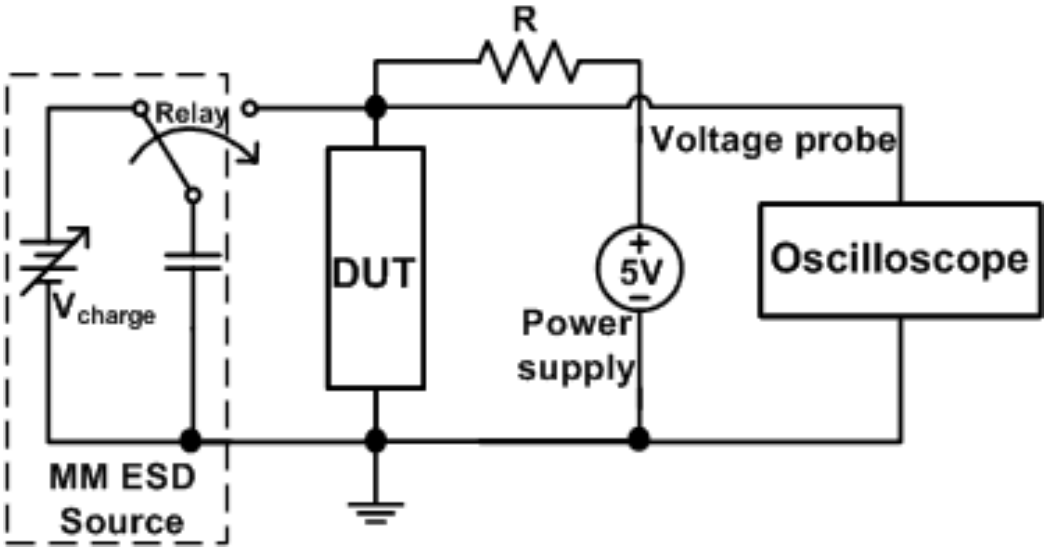


Fig. 4.34 Measurement setup of transient-induced-latchup (TLU) test [39].

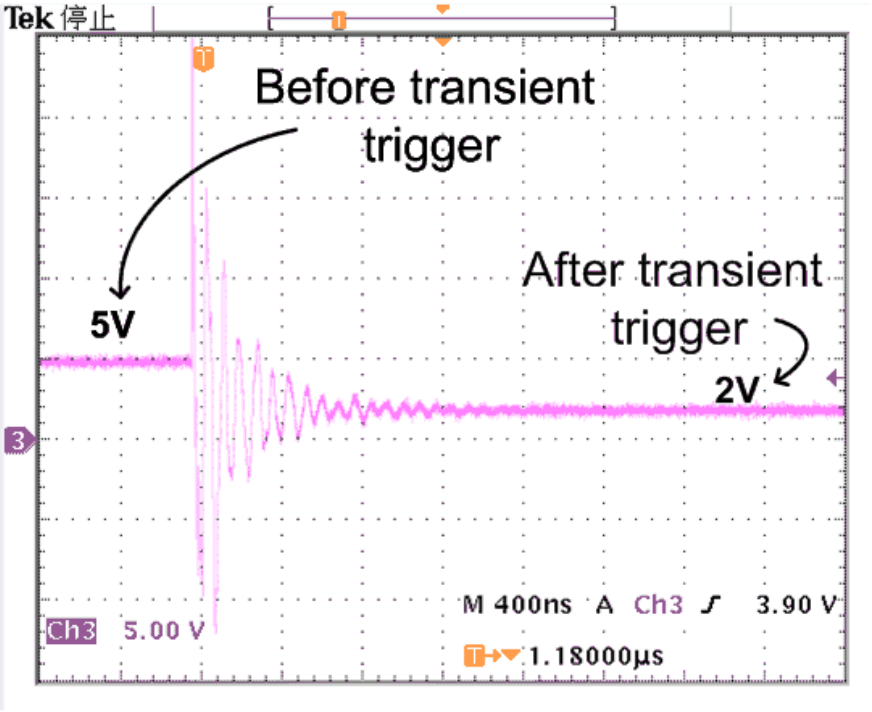


Fig. 4.35 Voltage waveforms before/after transient noise triggering on LVSCR-pnp.

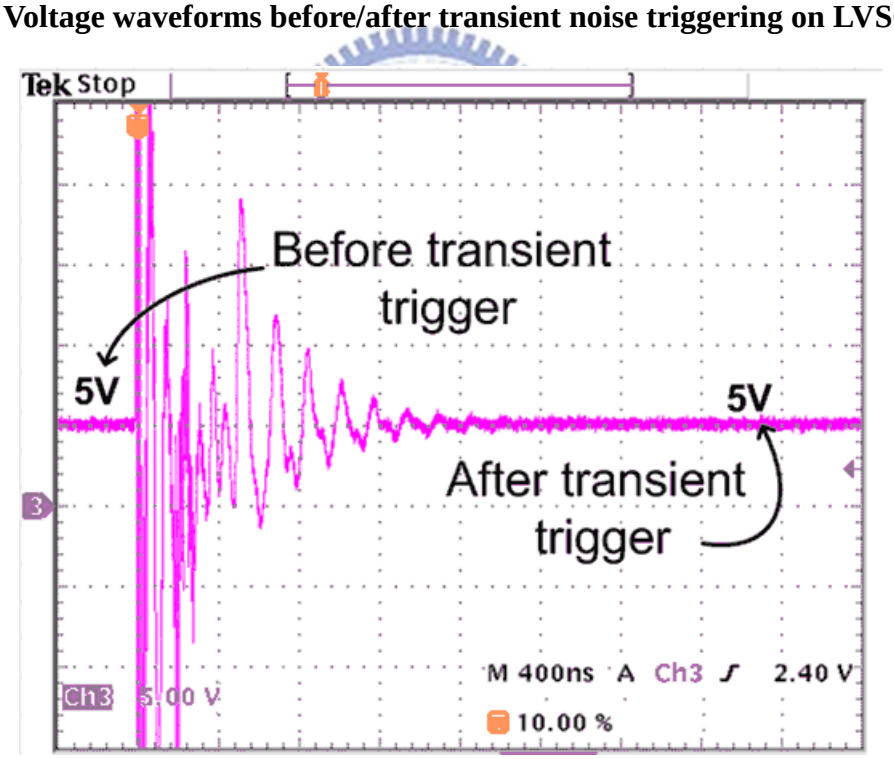


Fig. 4.36 Voltage waveforms before/after transient noise triggering on LVSCR-pnp+pn.

TABLE 4.1

The detail results of anode-engineering HVSCR.

Device name	Breakdown Voltage (V)	Trigger Voltage (Vt_1)	Holding Voltage (Vh)	It_2 Level	HBM
HVSCR-A-pn-ref	74 V	81 V	8.6 V	> 7 A	> 8 kV
HVSCR-A-pn	74 V	73 V	10.2 V	> 7 A	> 8 kV

TABLE 4.2

The comparisons of ESD robustness with in different implantation arrangement in anode.

Device name	Breakdown Voltage (V)	Trigger Voltage (Vt_1)	Holding Voltage (Vh)	It_2 Level	HBM
HVSCR-pnp-ref	74 V	74 V	6 V	> 7 A	> 8 kV
HVSCR-pnp-pn	41 V	74 V	13.4 V	1.5 A	5 kV
HVSCR-npn	97 V	108 V	13 V	3.9 A	> 8 kV

TABLE 4.3

The detail results of cathode-engineering in HVSCR.

Device name	Breakdown Voltage (V)	Trigger Voltage (Vt_1)	Holding Voltage (Vh)	It_2 Level	HBM
HVSCR-npn	97 V	108 V	13 V	3.9 A	> 8 kV
HVSCR-npn-SH_N	98 V	96 V	12 V	3 A	> 8 kV
HVSCR-npn-SH_N+pn	98 V	110 V	26 V	5.8 A	> 8 kV
HVSCR-npn-SH_N+pnsho	98 V	160 V	none	74 mA	0.5 kV
HVSCR-npn-SH_P-d35	98 V	125 V	21 V	> 7 A	> 8 kV
HVSCR-npn-SH_P+pn-d35	98 V	125 V	28 V	> 7 A	> 8 kV
HVSCR-npn-SH_P-dmin	47 V	86 V	17 V	6 A	> 8 kV
HVSCR-npn-SH_P+pn-dmin	47 V	87 V	28 V	> 7 A	> 8 kV

TABLE 4.4

The detail results of cathode-engineering in LVSCR.

Device name	Breakdown Voltage	Trigger Voltage (Vt_1)	Holding Voltage (Vh)	It_2 Level	HBM
LVSCR-pnp	18 V	22 V	3 V	> 7 A	> 8 kV
LVSCR-pnp+pn	18 V	22 V	7.7 V	> 7 A	> 8 kV
LVSCR-npn-H6	17 V	21 V	8 V	1.2 A	1 kV
LVSCR-npn+pn-H6	17 V	25 V	22 V	4 A	> 8 kV
LVSCR-npn-H10	17 V	26 V	24 V	3.5 A	6 kV
LVSCR-npn+pn-H10	17 V	29 V	27 V	2 A	3 kV

4.4.2 Summary

Owing to the discussion in this chapter, HVPB layer is the reason that causes the device premature failed. To let the device get in to snapback region successfully, removing the HVPB layer may help. The idea of additional p+ and n+ implantations will increase the holding voltage. Adding more implant layers in the cathode side in small device is more powerful, which means the holding voltage of the device that has additional n+ and p+ layers with small layout parameter increases more obviously. This method could get the same holding in relative low area consumption. However, when using this concept, the arrangement of n+ and p+ implant layers should be considered in HV process. If the p+ implant layer is close to the interface of HVPW and HVNW in both anode and cathode, this breakdown voltage lowering phenomenon would happen. Stretching the parameter of cathode to the edge of HVNW will change the breakdown voltage, trigger voltage, and holding voltage in the same time. Additional p+ and n+ method would only increase the holding voltage to a constant level regardless of the parameter. A designer could use this appearance to choose the suitable layout parameters for the high voltage application. In LVSCR, changing the parameter of cathode to the edge of N-type well only affects trigger voltage and holding voltage, especially the holding voltage. For the LV circuit in HV process, LVSCR-pnpdevice has been proved to be an excellent ESD protection device with high latchup-immune device. Also the device LVSCR-npn-H10 or LVSCR-npn+pn-H6 is suitable for stacking due to their weak snapback appearance. Stacking such devices may get the perfect ESD protection cell for power clamp in 40-V or 60-V application.The illustrations of stacking different number of devices and anticipation of the TLP resultsare shown in Fig.4.37. Hoping that stacking three LVSCR of LVSCR-npn-H10 or LVSCR-npn+pn-H6 could perfect fit ESD design window in Fig. 4.37(D).

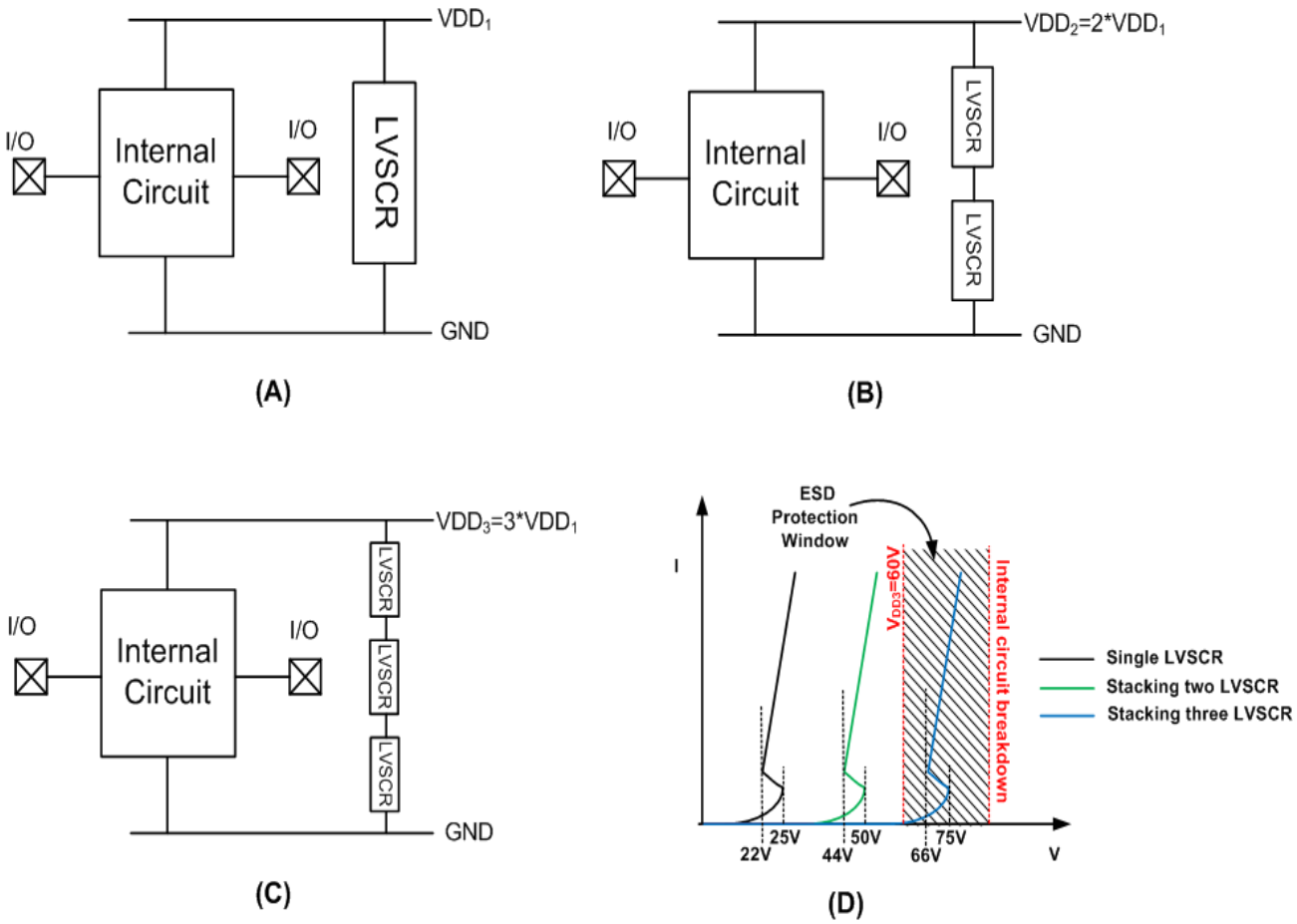


Fig. 4.37 (A) The illustration of LVSCR which can be used in 1*VDD circuit. (B) Stacking two LVSCRs can be used for 2*VDD circuit as a power clamp. (C) Stacking three LVSCRs in the circuit that operation voltage is VDD_3. (D) Stacking LVSCR can fit different operation condition in HV process. In the LVSCR-npn+pn-H6 case, stacking three devices would let the holding voltage become 66V and trigger voltage is 75 V which may prefect fit ESD design window.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis, various ESD protection devices have been proposed and fabricated in the test chip. The breakdown voltage, trigger voltage, and holding voltage are measured by the 100-ns TLP system. Those measurement results are reported and discussed in the relative section.

In Chapter 3, there are many different structures of nLDMOS realized in 0.25-μm 60-V BCD process. Those devices are designed for investigating different layout style, different parameter, different total width or different implant layers. The ESD robustness of nLDMOS is not scalable in this process which means increasing the total width is not an efficient way to improve the ESD performance. Changing the NBL layout style to non-fully isolate can let the device difficult to turn on. Changing the parameter of STI should combine with the proposed drain-side engineering. Only using both changes together would let the device snapback successfully and reaches a higher ESD levels.

To prevent the latchup issue, many different method of increasing holding voltage have been discussed in Chapter 4. The conjecture that HVPB layer is the reason that causes the device premature failed. The idea of additional p+ and n+ implantations will only increase the holding voltage, especially in the cathode side and in small device. Stretching the parameter of cathode to the edge of HVNW will change the breakdownvoltage, trigger voltage, and holding voltage in the same time. A designer can design a suitable device for the application by those appearance.

Furthermore, the weakly snapback LVSCR have been proposed. Stacking those devices is another choice to find a perfect ESD protection cell for power clamp in 60-V application. Also, for the LV circuit in HV process, the device LVSCR-pnp has been proved to be an excellent ESD protection device with high latchup-immunity.

5.2Future Work

Though there is a structure that has both good ESD protection abilities and latch up immunity in LV circuit. No structure can meet those constrains of ESD protection window as apower clamp in high voltage system. A good ESD robustness is not the only target. To be an ideal power clamp, the device should also have low trigger-on-voltage,which relates tohigh immunity for latchup, and enough margin for reliability under high voltage operation, which means that device's holding voltage should higher than the normal operation voltage. Theholding voltage ofthose devices,which have been proposed with good ESD robustness in this work, is still too low to be latchup-free, particularly of those structures with embedded SCR.

However, the ESD performance for nLDMOS depends on the process very much in high voltage process. The design of new device with the characteristics of both high holding voltage and high ESD robustness is still a challenge in the future.To find out a general ESD solution, there are two approaches. One is using the ESD detection circuit. The other way is stacking some ESD protection device to meet the constraints of ESD design window. Stacking many ESD protection devices would increase the breakdown voltage, trigger voltage, and holding voltage.Thus, decreasing the difference among these three kinds of voltages is the chance to get a perfect power clamp device in high voltage process.

In stacking configuration topology, the appropriate trigger voltageand holding voltage are very important. So, the deep investigation of LVSCR and HVSCR is needed. In the future, lower HVSCR trigger voltage is one of the options. Otherwise,

stacking the weakly snapback LVSCR is another approach.

Even though there are some weakly snapback LVSCRs, whichhave been proposed in this work, can be used asa stacked device. There is still some challenge of scalable increasing in the holding. Non-uniform triggering among BJT inherent in the high voltage ESD is another concern. So the realization of stacking structure is an important work in the future.

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