國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

100至200伏特SOI製程

高壓積體電路之靜電放電防護設計

On-Chip ESD Protection Design for High-Voltage ICs

in 100 ~ 200V SOI Process

研 究 生: 黃義傑　　(Yi-Jie Huang)

指導教授: 柯明道教授 (Prof. Ming-Dou Ker)

中華民國一○四年九月

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碩士論文

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高壓積體電路之靜電放電防護設計

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摘要

現今智能電源技術已經發展並且電子產品中很多積體電路是在高壓（HV）製程中被製造。例如車用 IC 等，通常使用高壓製程，與低壓（LV）元件相比，高壓電晶體結構較為複雜，這是為了放大操作範圍和崩潰電壓，如此一來使得靜電放電（ESD）防護的設計更加困難和具有挑戰性。

在高壓的靜電放電防護設計中，常會使用橫向擴散電晶體 (lateral diffused MOS, LDMOS)，這是常見的高壓電晶體，且與低壓電晶體相比，在同樣的布局大小下，通常高壓靜電防護元件的靜電耐受度表現較差，所以使用高壓防護元件，通常都會放大元件大小以達到要求的靜電耐受度，並且要特別注意均勻導通性。

高壓應用之靜電防護元件提出利用低壓 P 型場氧化層元件 (LVPFOD) 堆疊的構造在 0.5 微米高壓絕緣層覆矽 (silicon on insulator, SOI) 製程實現。在面積與靜電防護耐受度的考量下，低壓的靜電防護元件，在單位面積下，有比較好的靜電防護耐受度，使用堆疊方法使整體的導通電壓 (trigger voltage) 與持有電壓 (holding voltage) 往上疊加，使它滿足高壓積體電路的需求，所以堆疊可以是最佳的方法之一。在高壓靜電放電防護設計中，持有電壓是一個重要的考量，當在靜電防護元件的持有電壓低於供給的電壓時，在應用上有可能會發生閂鎖效應 (latchup)。實驗並驗證不同堆疊個數的低壓 P 型場氧化層元件在高壓應用下可以達到較高的靜電防護耐受度，並且達到閂鎖效應免疫。

在此篇論文中，探討了堆疊的靜電防護元件電阻值大小對人體模型和機器模型電流波形的影響效應，這解釋了堆疊的靜電防護元件電阻對峰值電流和波形震盪的影響非常明顯，特別是在機器模型的測試中。因為機器模型中的負載電阻主要受到堆疊的元件影響，但是人體模型則是受到 1.5 千歐姆的負載電阻影響，所以機器模型量測到的靜電防護耐受度隨著堆疊的低壓 P 型場氧化層元件個數增加而增加，而人體模型的靜電防護耐受度則不會隨著堆疊個數而改變，量測到相同的靜電防護耐受度。

On-Chip ESD Protection Design for High-Voltage ICs in 100 ~ 200V SOI Process

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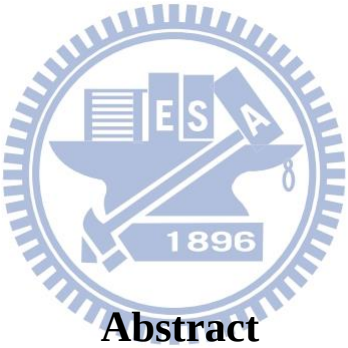

Abstract

Nowadays, the smart power technology has been developed and many integrated circuits (ICs) of electrical products fabricated in a high-voltage (HV) process. Automotive ICs, power management ICs, and driver ICs for various display panels are commonly fabricated in a HV process. HV transistors are fabricated with complicated structure for enlarging the operating range and breakdown voltage, and that makes electrostatic discharge (ESD) protection design more difficult and challenging compared with the low-voltage (LV) devices.

In ESD protection design for HV applications, it is common to use lateral diffused MOS (LDMOS) as an ESD protection device. LDMOS is a general HV transistor in a HV process, and its ESD robustness is worse than a LV device's. Enlarging LDMOS's total width can

increase ESD robustness, but it should be aware of uniformity for ESD protection.

In this thesis, ESD protection with LV p-type field-oxide devices (LVPFOD) in stacked configuration is proposed for HV applications in a 0.5-μm HV SOI process. For area and ESD robustness concerns, LV devices are proved with good ESD robustness per area. Stacking increases trigger voltage and holding voltage so that the devices meet the conditions. Therefore, stacking can be one of the best ways for ESD protection in HV applications. In ESD protection design for HV applications, holding voltage of a device is an important factor. When holding voltage of a device is lower than supply voltage, it is possible that latchup occurs in applications. Stacked LVPFOD with different stacking numbers have been verified in silicon chip to exhibit both of high ESD robustness and latchup-free immunity for HV applications.

In this thesis, the effect of the stacked ESD protection device's resistance on Human Body Model (HBM) and Machine Model (MM) current waveform is studied. It is shown that the stacked device's resistance can have a significant impact on the peak current and damping waveform, especially for MM ESD test. Because the load resistance of MM is dominated by stacked device and the HBM is dominated by 1.5 kΩ, the MM ESD level increases by the numbers of stacked LVPFOD, and all the HBM ESD level are the same.

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黃義傑

104 年 9 月於竹塹交大

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Chapter 1
Introduction

1.1 Motivation

The smart power technology has been developed and many integrated circuits (ICs) of electrical products are fabricated in a high-voltage (HV) process. More and more HV applications are flourished in commercial ICs such as automotive ICs, power management ICs, and driver ICs, which were often realized with the Laterally-Diffused-MOS (LDMOS) devices [1], [2]. With development of high-voltage technology, electrostatic discharge (ESD) protection in HV ICs products should be provided for the need. However, ESD protection device in HV applications still faces some problems.

The HV ICs implemented in the SOI process have got more advantages to manage HV blocks, to reduce parasitic bipolar effect and increase circuit speed. To get sufficient ESD robustness for the HV ICs, the HV devices at the I/O pins were often drawn with a large device dimension to meet the ESD specifications. High-voltage pins of ICs should have special ESD protection devices for their high operation voltage. Modifying typical HV MOSFETs is a choice for ESD protection. However, high-voltage devices such as LDMOS are usually inherent weak at ESD robustness because of non-uniform turn-on phenomenon [3]. It will take times to improve ESD robustness of high-voltage devices and make optimization by lots of splits.

In the literatures [4]-[11], ESD protection in SOI process was reported with MOS and silicon controlled rectifier (SCR) combining together into the same device structure, which allowed SCR being triggered on to reach a high ESD robustness. However, the holding voltage (V_h) of SCR was much lower than the circuit operation voltage level, that it would cause serious latchup-like failure issue in the HV applications. Comparing to HV devices, the

LV devices were relatively good at ESD robustness, and the stacked configuration is a way to achieve a high V_h [12].

In this thesis, the stacked low-voltage p-type field-oxide devices (LVPFOD) with different stacking numbers for HV applications were investigated in a 0.5-μm SOI process. In a 0.5-μm SOI process, the operation voltages focus on 120 V, 150 V and 200 V. Different HV ESD protection devices were also accomplished as reference. Experimental results measured by DC I-V curve tracer, transmission-line-pulsing (TLP) system, and ESD tester have confirmed that the proposed solution can achieve both of high ESD robustness and latchup-free immunity for HV applications.

To examine Human Body Model (HBM) and Machine Model (MM) effect on stacked ESD protection device, methods with peak current (Ipeak) test had been defined in JEDEC standards [13]-[15]. It is suggested that ICs should require 2 kV in HBM and 200 V in MM. TABLE 1.1 is the characterization of the peak current for short circuit HBM and MM ESD test specified in the up-to-date JEDEC standards. In the literature [16], the effect of the sensor resistance on HBM and MM ESD current waveform is studied. The MM ESD level increases by the device resistance with different stacking numbers. By measuring the peak current of current waveform knows that the resistance trend with different stacking numbers. In this work, it shown that the device resistance can have a significant impact on the peak current, especially for MM ESD test.

1.2 Typical ESD Protection Design Scheme in High-Voltage Integrated Circuits

The locations of the ESD protection circuits to achieve whole-chip ESD protection for CMOS ICs is shown in Fig. 1.1. Each I/O pin should have ESD protection devices to construct two paths to power line and ground line, and the power rail clamp should provide an ESD path from Vcc to ground. The whole-chip ESD protection can protect ESD event, when

ESD happen at fabrication, transportation, package and assembly processes. If no protection devices in ICs, ICs may burn out and losing their functionality. ESD plays an important role in the reliability issue on the semiconductor industry.

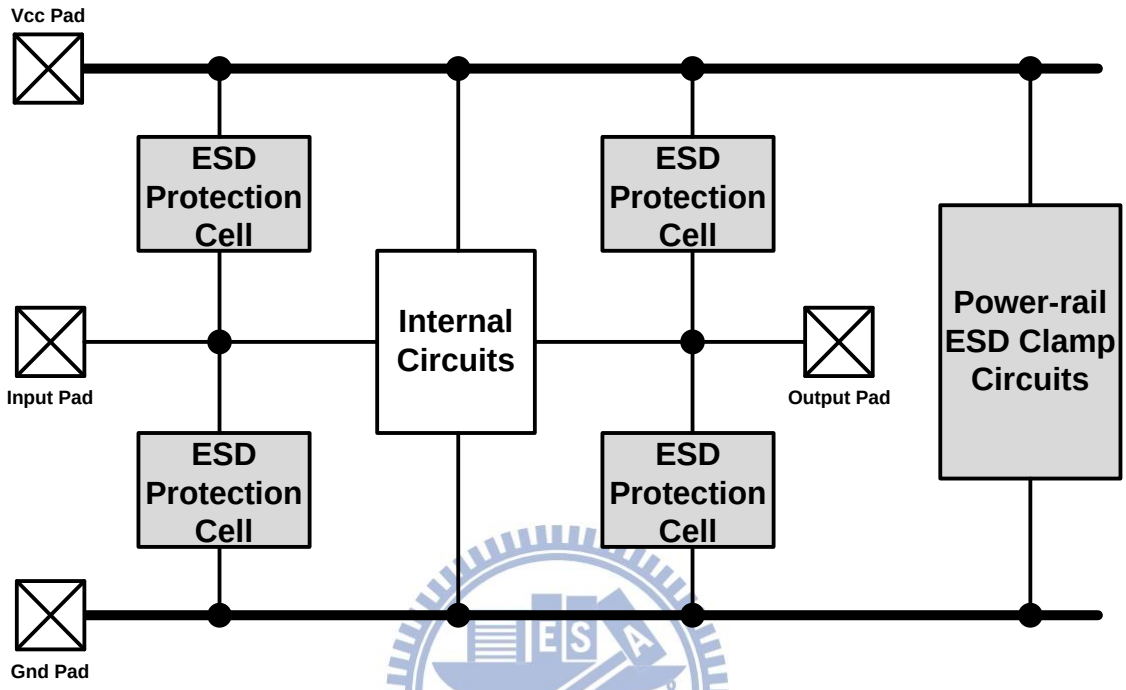


Fig. 1.1 A typical whole-chip ESD protection scheme.

TLP is common system in ESD protection study because the system provides more details about the I-V characteristic of the device. In Fig. 1.2 [2], there is an I-V curve measured by TLP systems. And it shows ESD protection design window of ESD protection device. Trigger voltage represents the triggering of parasitic BJT, which is needed below the gate oxide breakdown voltage of internal circuit. The holding voltage is the lowest voltage after parasitic device triggering, which should higher than the supply voltage. Second breakdown current (I_{t2}) is the maximum current handling ability of the device. The device will be failure after I_{t2} point. The TLP result is corresponding to HBM ESD level in low-voltage application, but it has no connection in high-voltage application.

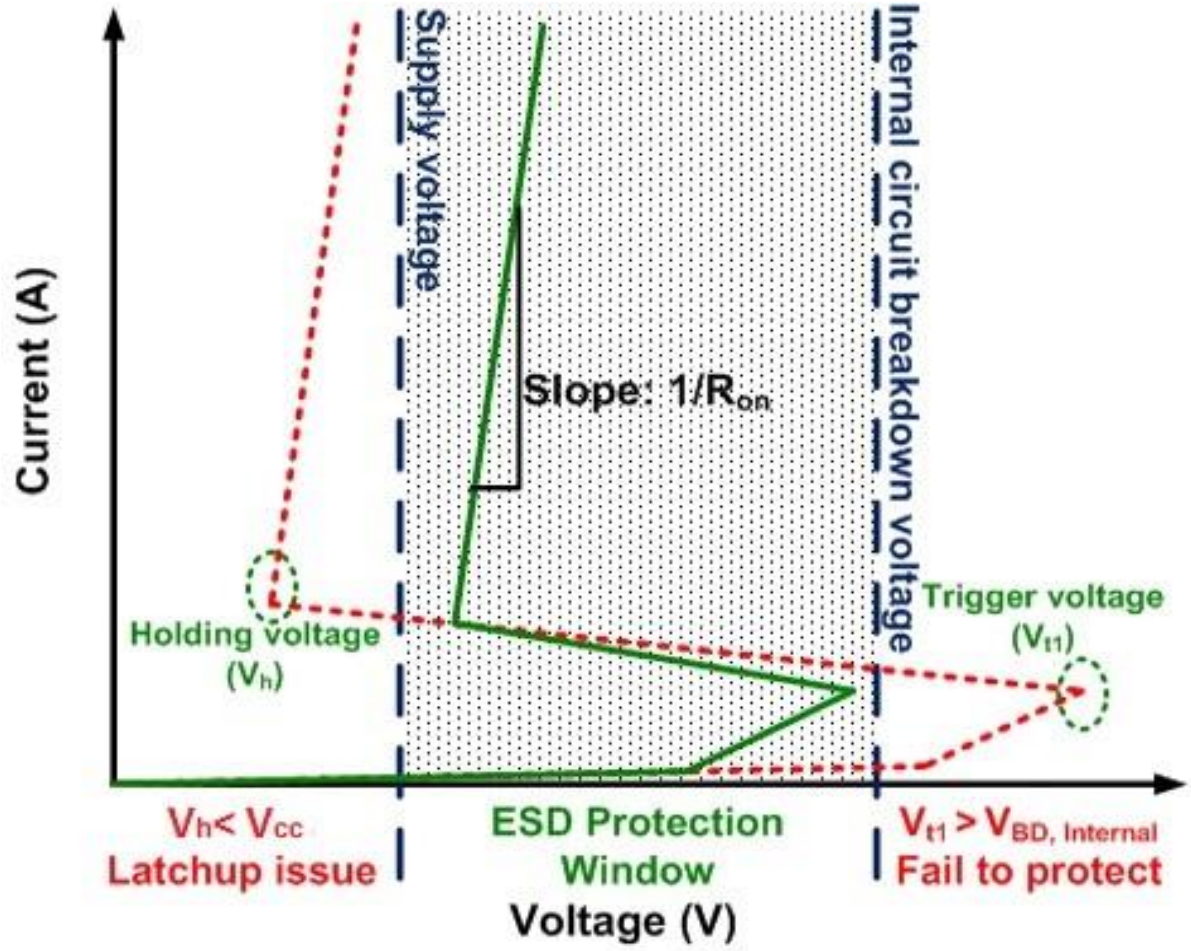


Fig. 1.2 I-V characteristic of ESD protection device to meet ESD protection window [2].

1.3 Latchup Issue in High-Voltage ESD Protection

The latchup issue [17], [18] is one of the most critical issues in high-voltage ESD protection. Latchup issue is more serious than in low-voltage operation. Ideal ESD protection devices should have low trigger voltage, high holding voltage for latchup immunity. In HV process, the nLDMOS has much lower holding voltage than the supply voltage, not to mention the embedded SCR structure. One condition for latchup occurred is that the holding voltage below the supply voltage. Another condition is that the power supply current should be large enough to support the holding condition. Therefore, the solution to improve latchup immunity is to increase the holding voltage. Also reducing the supply current is the one way, but sometimes lower supply current would reduce the performance.

As shown in Fig. 1.3(a) and 1.3(b), the parasitic circuit includes two BJTs (one is NPN, the other is PNP) and two resistances (one is Rwell, and other is Rsub). The SCR is two terminals and four layers P-N-P-N (P+/Nsub/Pwell/N+) structure. When a positive voltage applied on the anode of SCR is larger than the breakdown voltage and the cathode is relatively grounded. The TLP I-V characteristic of SCR is shown in Fig. 1.4. The positive feedback generated by the large enough substrate or well current of SCR structure. If the voltage drop across the resistance is larger than 0.7-V, the parasitic BJT will be turn on and initiates the SCR into latchup state. When latchup happens, the current will conduct through a low impedance path from the power supply to ground. The current is not limited, irreversible damage will happen by the high power. In order to avoid the latchup effect, silicon on insulator (SOI) is one of the methods to overcome latchup, which was fully isolated to each other by the deep trench isolation (DTI) and buried oxide.

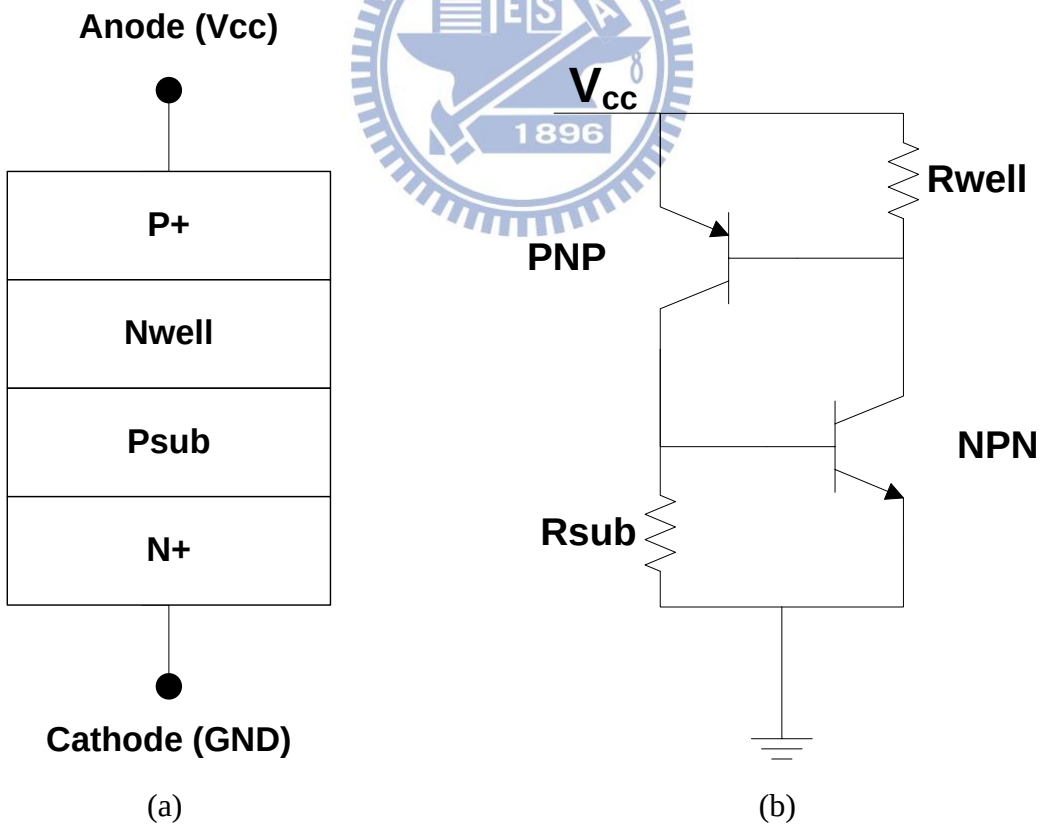


Fig. 1.3 (a) Two terminals and four layers P-N-P-N, and (b) Equivalent circuit of SCR.

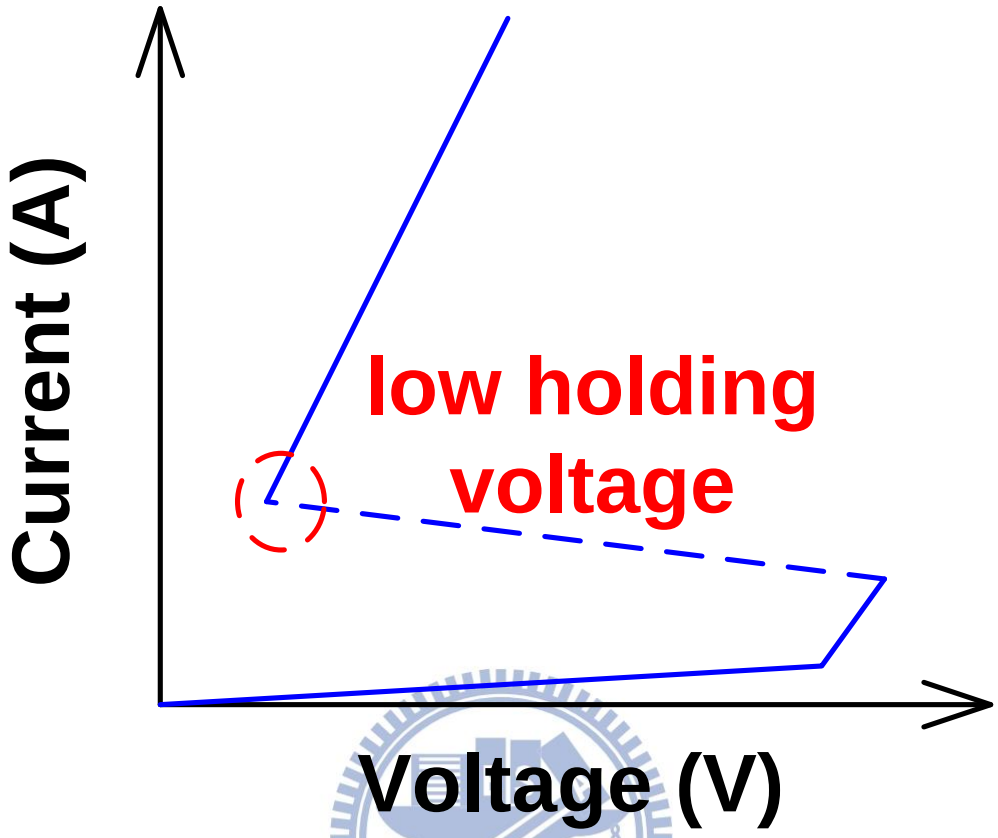


Fig. 1.4 TLP I-V characteristic of SCR.

1.4 HBM and MM Measurement Methods

Human Body Model (HBM) and Machine Model (MM) are two different conditions and sources of ESD. ESD robustness can be tested in several ways, there are HBM and MM ESD test standards [13], [14]. As shown in TABLE 1.1, the HBM and MM wave form specification are defined, which was used the shorting wire in ESD test standards. The tester must meet the requirements of TABLE 1.1. The waveform specifications listed in this table remain valid and shall be examined for compliance in tester qualification, calibration and waveform verification.

TABLE 1.1

HBM and MM Waveform Specification [13], [14].

HBM Voltage Level (V)	Ipeak for Short (A)
250	0.15 – 0.19
500	0.30 – 0.37
1000	0.60 – 0.74
2000	1.20 – 1.48
4000	2.40 – 2.96
8000(optional)	4.80 – 5.86
MM Voltage Level (V)	Ipeak for Short (A)
100	1.5 – 2.0
200	2.8 – 3.8
400	5.8 – 8.0

HBM is one of common ESD events. The HBM ESD event arises from the connection of a charged human body and an IC product. The typical equivalent HBM ESD circuit is shown in Fig. 1.4. In typical equivalent HBM ESD circuit, a 1.5 kΩ resistor and a 100 pF capacitor are placed to represent the parasitic resistor and capacitor of a human body. It is generally required 2 kV in HBM. As shown in Fig. 1.5, current waveform of HBM ESD stress discharging through a short wire. It defines the HBM pulse decay time (td).

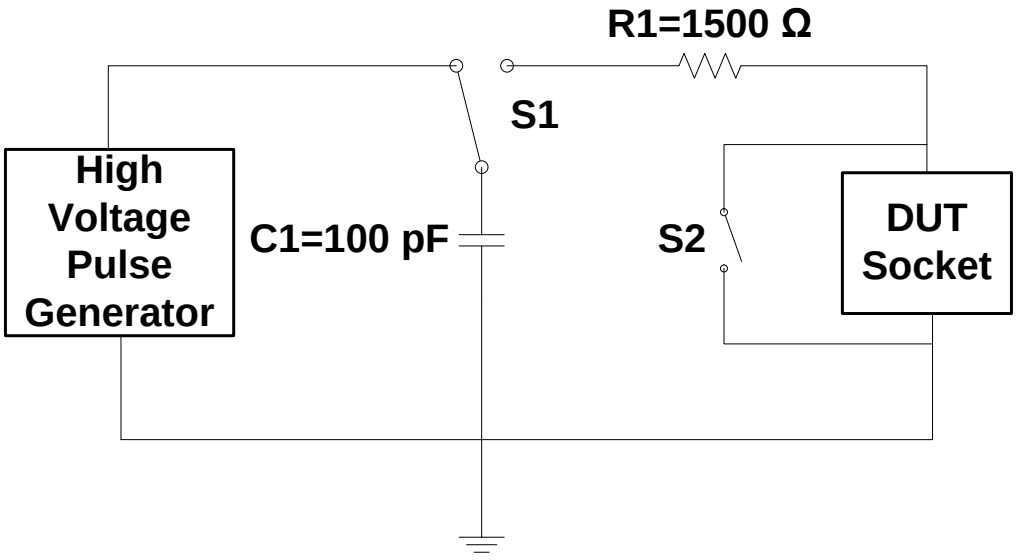


Fig. 1.5 Typical equivalent HBM ESD circuit [13].

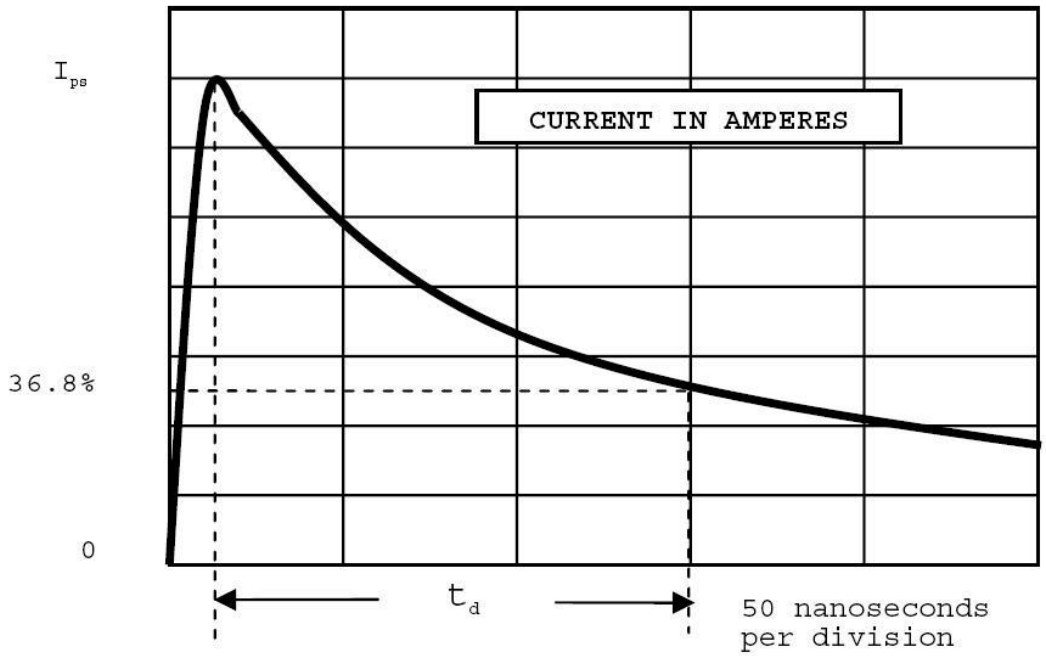


Fig. 1.6 Current waveform of definition of the HBM pulse decay time (td) through a short wire [13].

MM is another of common ESD events. MM ESD event arises from the connection of a machine and an IC product. The typical equivalent MM ESD circuit is shown in Fig. 1.6. There is no equivalent resistor on the discharging path. It is generally required 200 V in MM. As shown in Fig. 1.7, current waveform of a 400 V MM ESD stress discharging through a short wire.

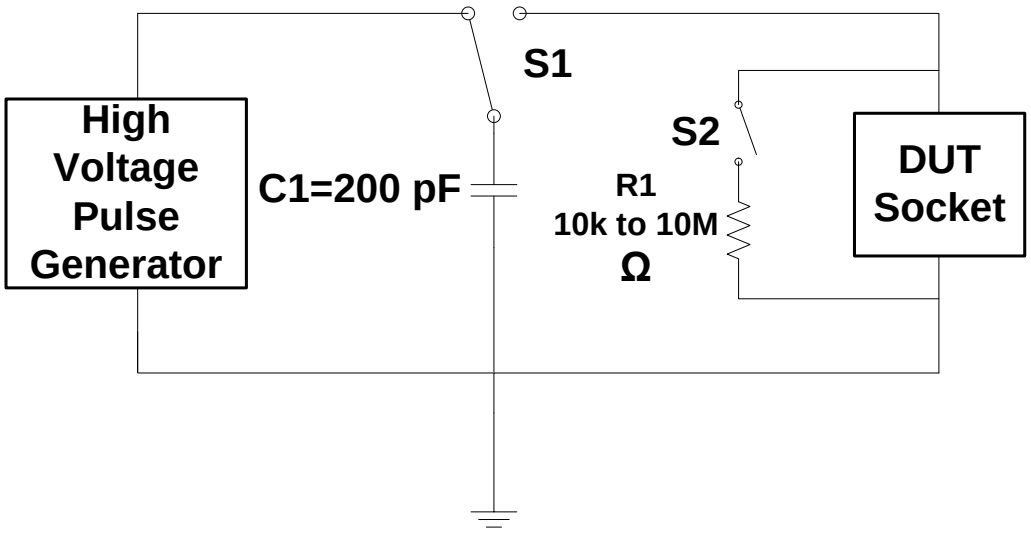


Fig. 1.7 Typical equivalent MM ESD circuit [14].

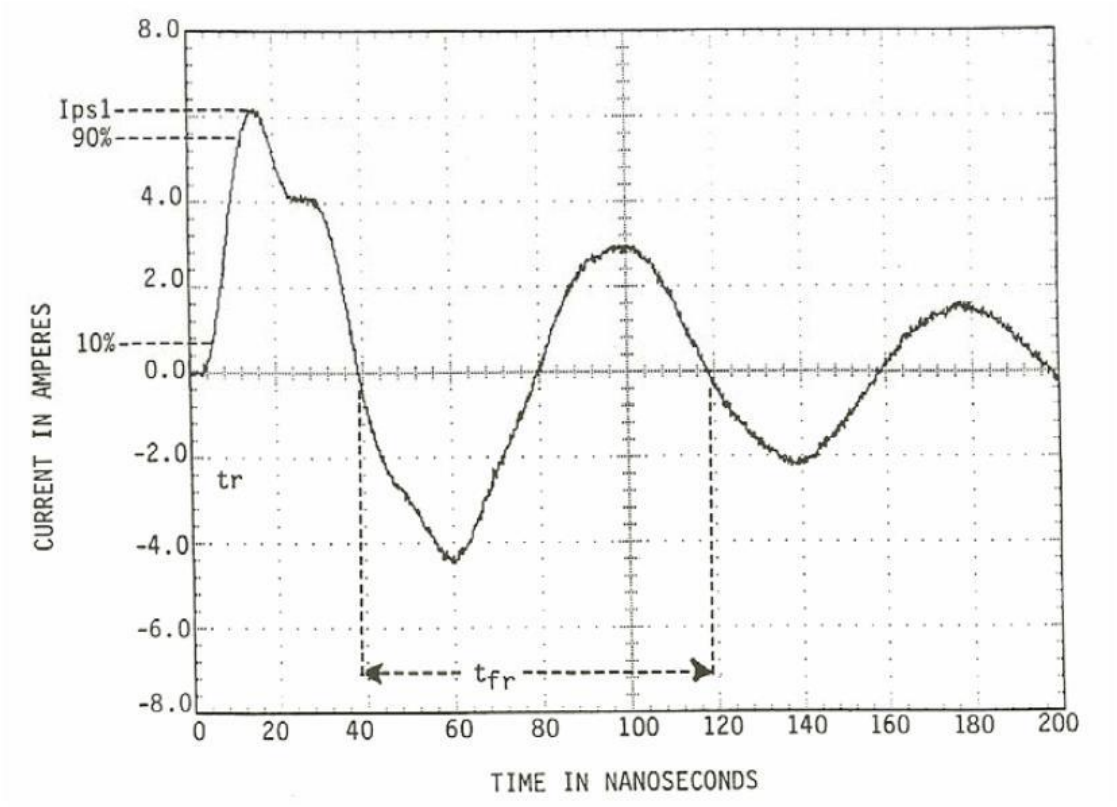


Fig. 1.8 Current waveform of a 400 V MM ESD stress discharging through a short wire [14].

1.5 Thesis Organization

This thesis focuses on stacked devices in a SOI process for high voltage ESD protection with latchup-free immunity. Also focuses on Human Body Model and Machine Model effect on stacked ESD protection devices.

In chapter 1, it introduces research motivation, measurement methods, a typical protection scheme and the thesis organization. It describes prior arts, and studies stacked low-voltage device characteristics in chapter 2. Chapter 3 shows stacked low-voltage and high-voltage device characteristics. In chapter 4, an experiment is investigated of Human Body Model and Machine Model effect on stacked ESD protection devices for high-voltage application. In the last chapter, the conclusions and some suggestions for future work have been discussed.

Chapter 2

Prior Arts and Stacked Low-Voltage Devices

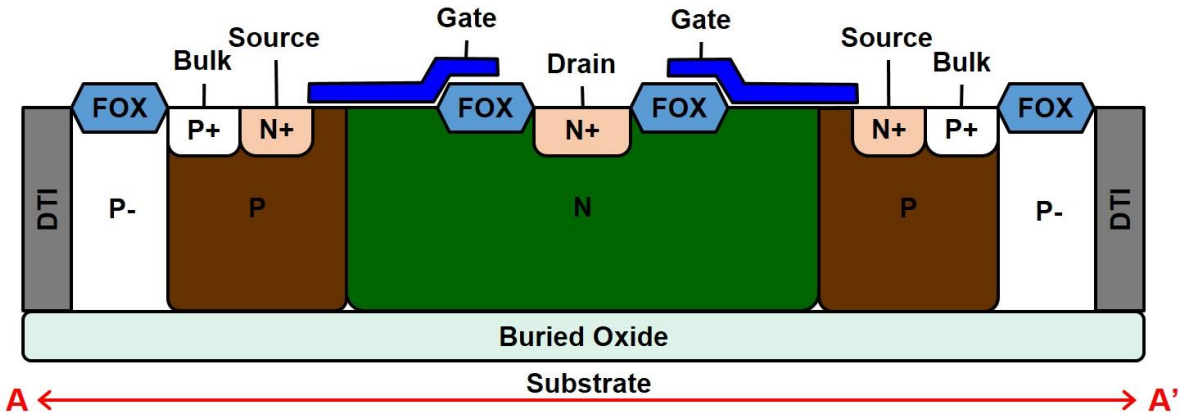
2.1 Prior Arts

There are many ESD solutions for HV ESD protection in SOI process [4]-[11]. ESD protection in SOI process was reported with MOS and SCR combining together into the same device structure, which allowed SCR being triggered on to reach a high ESD robustness. However, the holding voltage (V_h) of SCR was much lower than the circuit operation voltage level, that it would cause serious latchup-like failure issue in the HV applications. High-voltage pins are sensitive to latchup issue. Modified n-channel LDMOS or HV silicon-controlled-rectifier (HVSCR) suffer this latent latchup problem due to their low holding voltage. The typical I-V characteristic of ESD protection device is shown in Fig. 1.2. ESD protection devices can be totally latchup-free by increasing holding voltage over supply voltage. The snapback behavior of the SCR embedded with HV nLDMOS together is still not fulfilled ESD design window for HV applications. Comparing to HV devices, the LV devices were relatively good at ESD robustness, and the stacked configuration is a way to achieve a high V_h [12]. The end of this chapter will compare with HV ESD protection solutions among the prior arts and proposed 12-LVPFOD stacked in SOI process. The silicon data shows that stacked LVPFOD applied for 120V application in SOI process can pass 4kV HBM level with reasonable layout area.

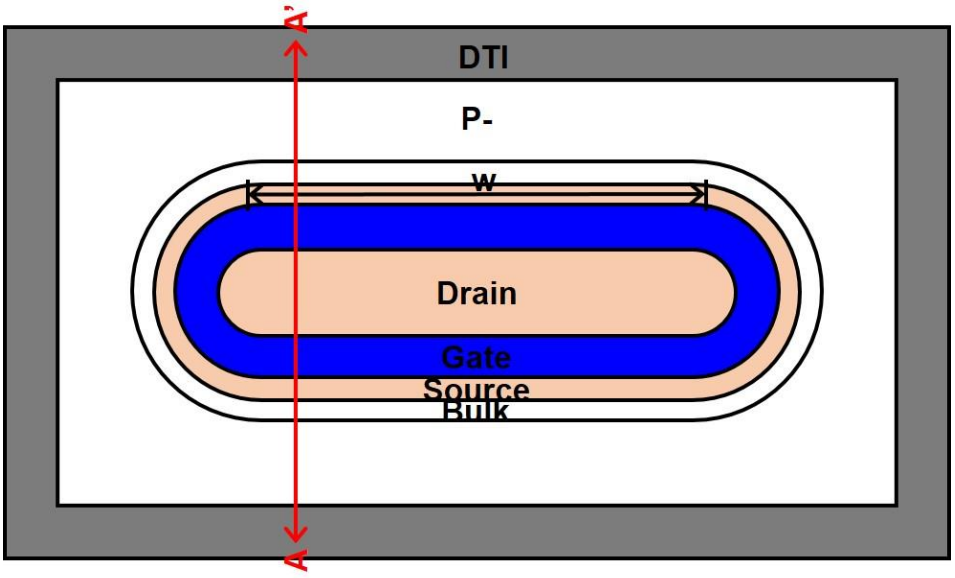
2.2 Typical HV SOI Devices

The simplified device cross-sectional view and the corresponding layout top view of the HV nLDMOSs are shown in Fig. 2.1 (a) and 2.1 (b), respectively. In SOI process, HV device structures are made like racetrack type. For 120 V, 150 V, and 200 V applications, the

changing of different operation voltage HV devices is to adjust design rule in the same structure. The width is defined by the straight line among racetrack type structure. The device dimension of nLDMOS was drawn as 2W = 200 μm and L = 2.78 μm in the testchip. They were fully isolated by the DTI and buried oxide. The typical devices of HV nLDMOS had been drown with minimum rule of the given SOI process.



(a)



(b)

Fig. 2.1 Device (a) cross-sectional view, and (b) layout top view of HV nLDMOS in a 0.5-μm SOI process.

The TLP-measured I-V characteristic of the 120 V, 150 V, and 200 V nLDMOSs are shown in Fig. 3. The drain breakdown voltage of the HV nLDMOSs are 147.0 V, 192.8 V, and

271 V, respectively. And the trigger voltage (V_{t1}) are 155.3 V, 206.3 V, and 275.5 V, respectively. But, such a HV device got a very low ESD robustness (<500 V for 120 V, 1 kV for 150 V and 200 V, HBM), which was almost burned out immediately when entering into its snapback region. The HV nLDMOSs cannot provide self-protection, but also unable to protect the internal circuits or devices in the HV ICs.

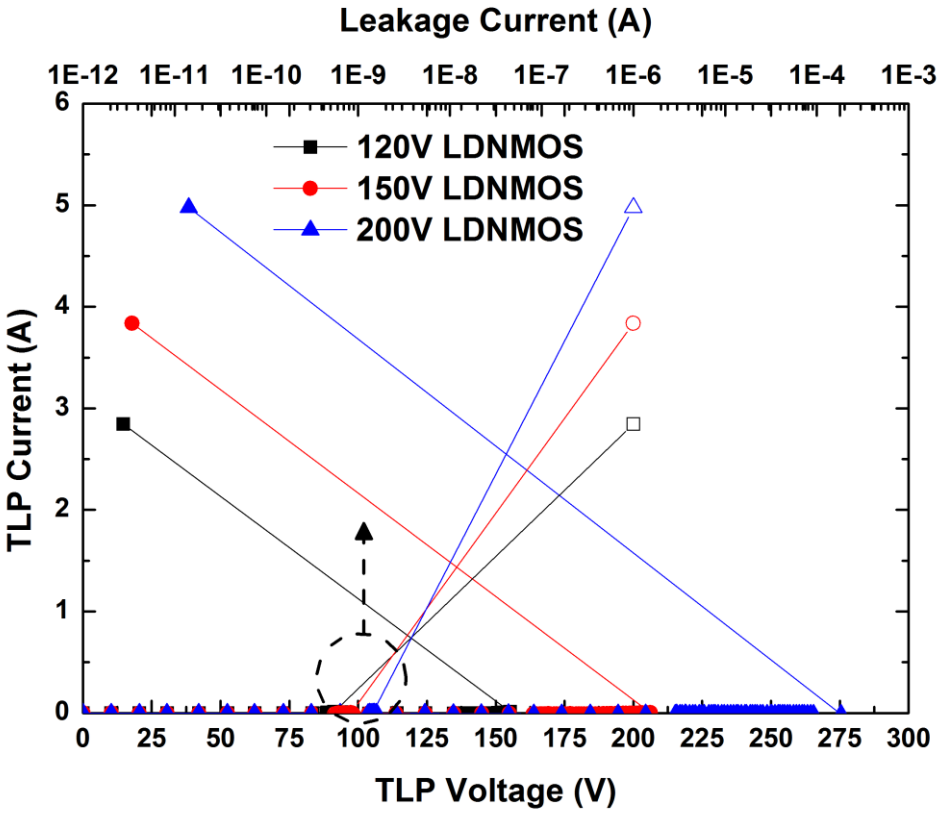


Fig. 2.2 TLP I-V characteristic of HV nLDMOSs in a 0.5-μm SOI process.

The detailed characteristic of HV nLDMOSs are listed in TABLE 2.1. HV nLDMOS breakdown voltage will be the internal circuit breakdown voltage for ESD protection design. As a result, ESD protection window can be defined clearly. To design the ESD protection devices, which adjusting trigger and holding voltage into the middle part of ESD protection window. It can not only protect internal circuit effectively, but also solve the problem for latchup-free immunity design.

TABLE 2.1
Summary of HV nLDMOS in a 0.5-μm SOI Process.

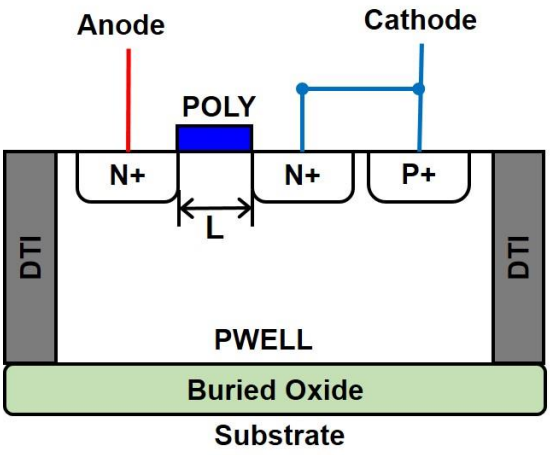
HV nLDMOS operation voltage	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*
120 V	155.26	N.A.	N.A.	147.0	<500
150 V	206.25	N.A.	N.A.	192.8	1
200 V	275.45	N.A.	N.A.	271.0	1

(*) ESD failure criteria : BV (I @1μA) shift >20%.

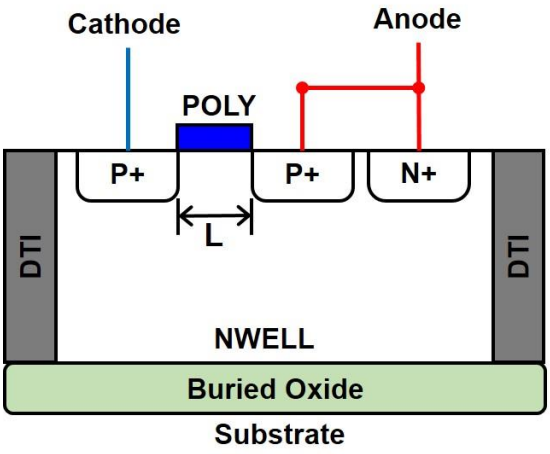
2.3 Low-Voltage Device Structures

In this chapter, the proposed solution will use the LV device structures. The device cross-sectional view is signification of LV device unit, as shown in Fig. 2.3. There are three kinds of LV devices, which are studied in this section (LVNMOS, LVPMOS, and LVPFOD, respectively). They are typical structure in SOI process. The dimensions for LV device unit were drawn with W = 800 μm and S = 0.5 μm for LVNMOS, W = 800 μm and S = 0.5 μm for LVPMOS, and W = 800 μm and S = 0.9 μm for LVPFOD. They were fully isolated by the DTI and buried oxide. All LV typical devices had been drawn with minimum rules of the given SOI process, expect the channel width (W). The drain breakdown voltage of the LV device unit are 11.5 V, 10.5 V, and 11 V, respectively.

The device cross-sectional view is signification of stacked LV devices, as shown in Fig. 2.4. Every LV device was only connected through the metal layers to make the stacked configuration with different stacking numbers. They were fully isolated to each other by the DTI and buried oxide. So it is possible to estimate the stacking number of LV device easily for different circuit operation voltage.



(a)



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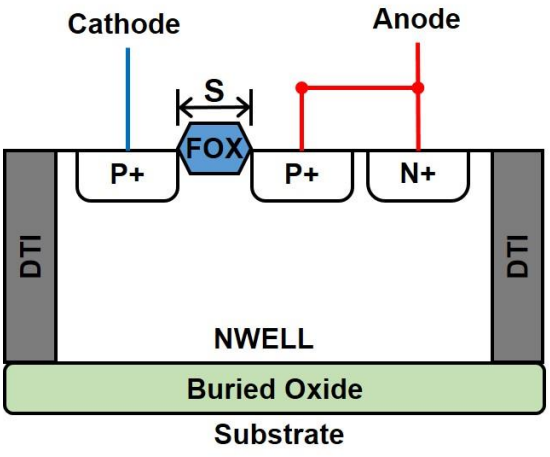
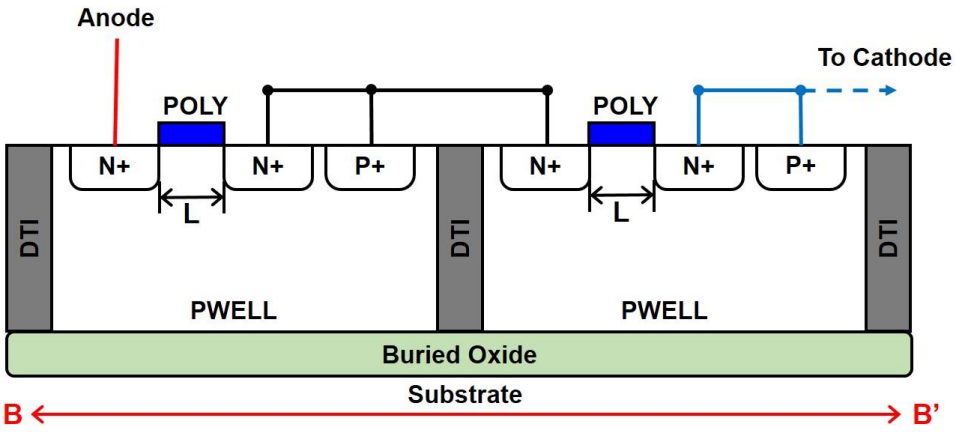
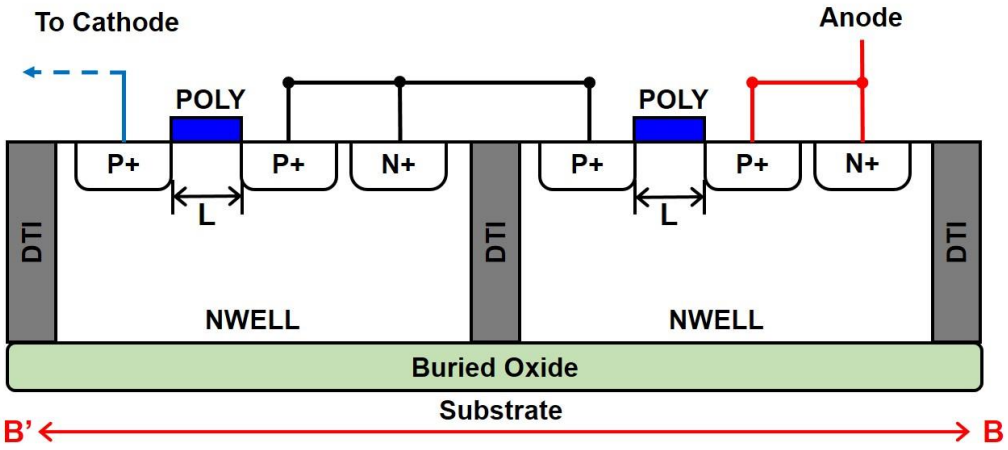


(c)

Fig. 2.3 Device cross-sectional view of (a) LVNMOS unit, (b) LVPMOS unit, and (c) LVPFOD unit, in a 0.5-μm SOI process.



(a)



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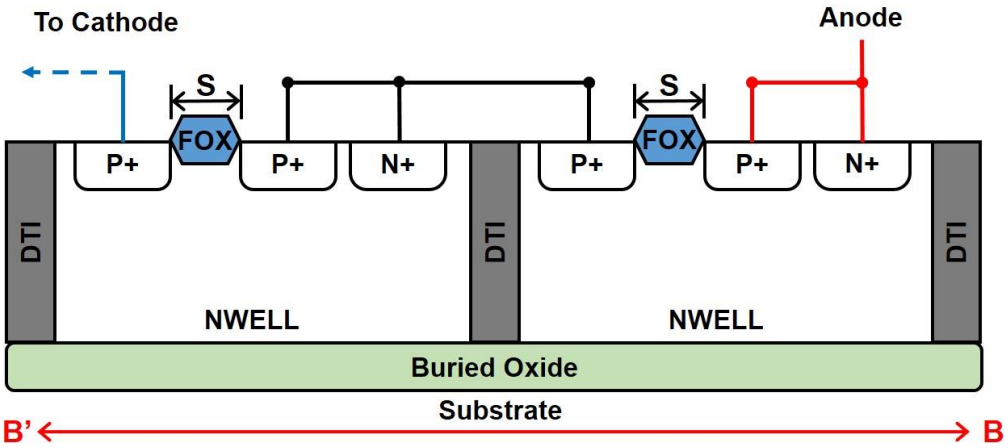


(c)

Fig. 2.4 Device cross-sectional view of stacked (a) LVNMOS, (b) LVPMOS, and (c) LVPFOD, in a 0.5-μm SOI process.

The device top view is signification of stacked LV devices, as shown in Fig. 2.5. Every LV device was only connected through the metal layers to make the stacked configuration with different stacking numbers. They were fully isolated to each other by the DTI and buried oxide. It is possible to estimate the stacked number of LV devices easily for different circuit operation voltage. It just shown the line configuration, and the shape of stacked is more flexible to fit into various layouts in folded configuration [19]. The different characteristic between two configurations is small. In this chapter, it is examined and compared in line configuration. But in next chapter, it would be in folded configuration.

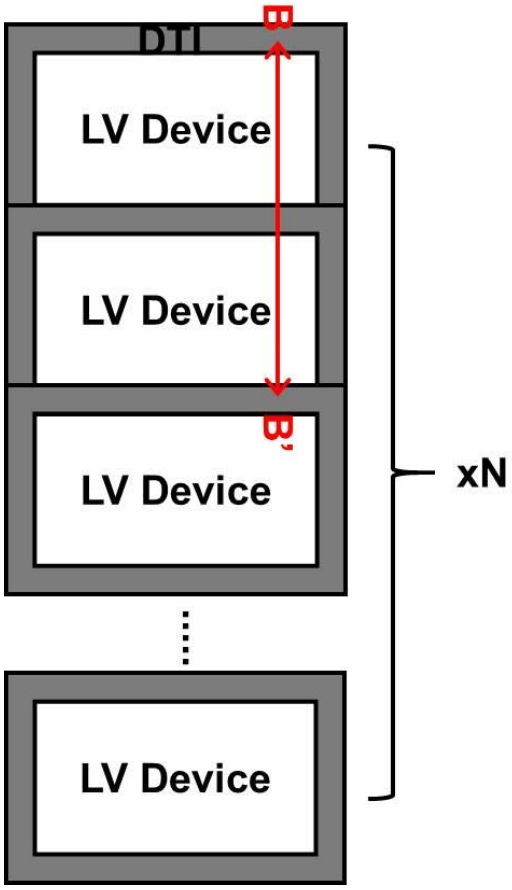


Fig. 2.5 A top view of stacked low-voltage device structure.

2.4 Low-Voltage Device Characteristics

2.4.1 Metal Routing

As mentioned in the previous section, there are metal routing of two configuration [19] as shown in Fig. 2.6. Only two metal layers were used in these devices. The metal routing and finger are perpendicular to each other, which is distributed current uniformly. The U turn metal also notice the metal width, and make current flow the same metal width. Stacked devices performed almost the same in the line and folded configurations. The trigger voltage, holding voltage, and second breakdown current keep the same values.

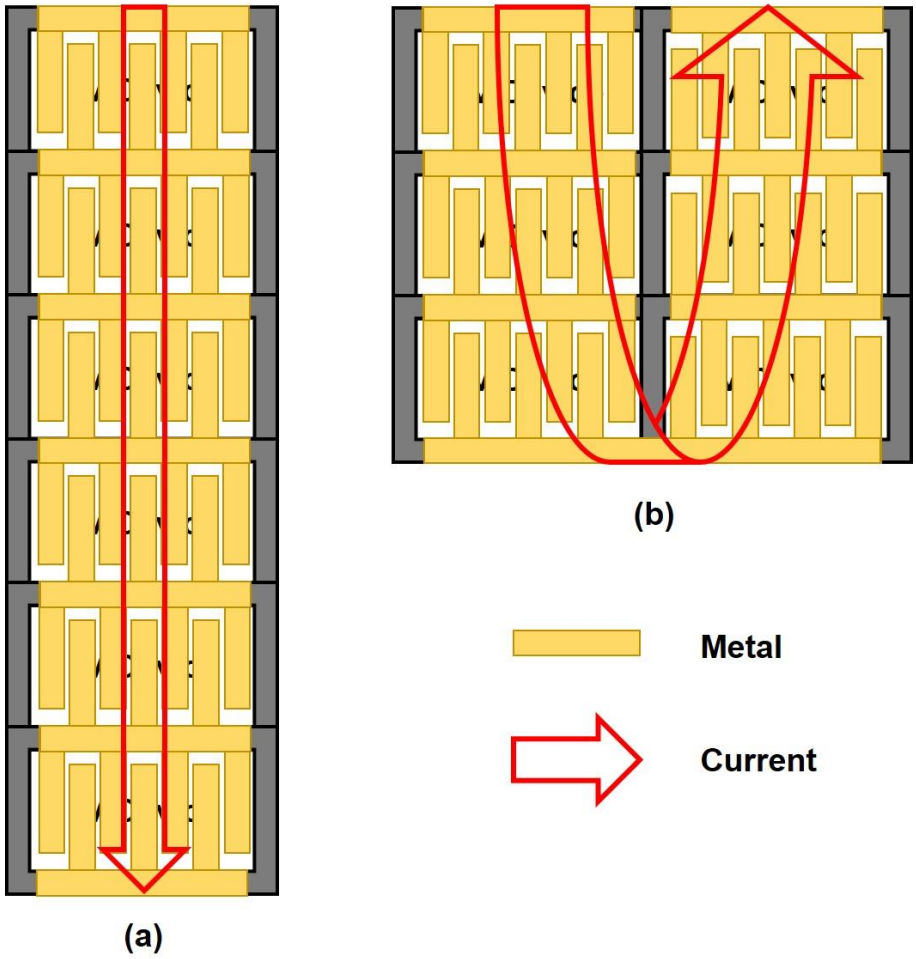


Fig. 2.6 Metal routing (a) in line configuration, and (b) in folded configuration [19].

2.4.2 Low-Voltage Devices

For LVNMOS, the device unit dimension was drawn as W = 800 μm and L = 0.5 μm. To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias is 10 V for each unit. The TLP-measured I-V characteristic of the LVNMOSs are shown in Fig. 2.7. The drain breakdown voltage of the LVNMOS unit is 11.5 V, and the trigger voltage (V_{t1}) is 12.30 V. LVNMOS can be stacked up for higher trigger voltage. But, such a LVNMOS got a very low ESD robustness, which was almost burned out immediately when entering into its snapback region. The most significant cause for bad ESD robustness is the multi-finger non-uniform turn-on issue.

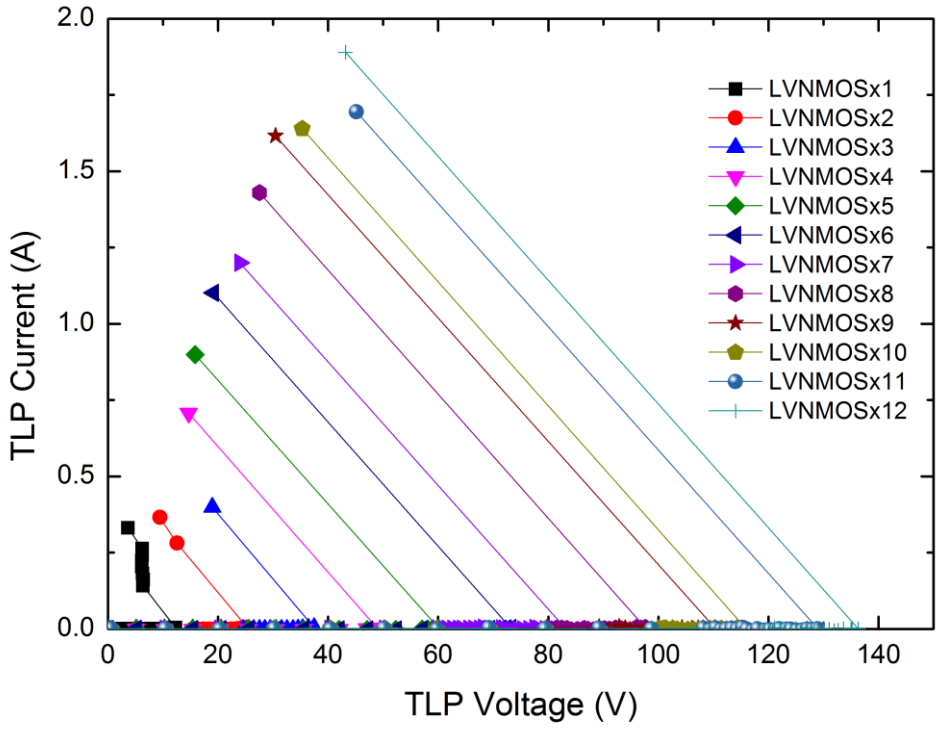


Fig. 2.7 Stacked LVNMOS TLP I-V curve characteristic.

The detailed characteristic of stacked LVNMOSs with different stacking numbers are listed in TABLE 2.2. By adjusting the stacking numbers, the trigger voltage can linearly increase. But the bad ESD robustness as shown in the table, the proposed ESD protection solution cannot be further used for higher voltage applications and not getting latchup-free immunity. Stacked LVNMOSs were almost burned out immediately when entering into its snapback region. LVNMOS is not a useable solution for latchup-free immunity design.

TABLE 2.2

Summary of Stacked LVNMOS TLP ESD Robustness with Different Stacking Numbers.

Stacked Number of LVNMOS	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*
1	12.30	3.63	0.26	11.5	0.5
2	25.26	9.45	0.28	22.5	<0.5
3	37.44	N.A.	N.A.	34.0	0.5
4	48.91	N.A.	N.A.	45.5	<0.5
5	60.10	N.A.	N.A.	56.5	<0.5
6	73.24	N.A.	N.A.	68.0	<0.5
7	83.22	N.A.	N.A.	79.0	<0.5
8	97.63	N.A.	N.A.	90.5	<0.5
9	110.28	N.A.	N.A.	101.5	<0.5
10	116.02	N.A.	N.A.	113.0	<0.5
11	128.93	N.A.	N.A.	124.5	<0.5
12	136.31	N.A.	N.A.	135.5	<0.5

(*) ESD failure criteria : BV (I @1μA) shift >20%.

For LVPMOS, the device dimension was drawn as W = 800 μm and L = 0.5 μm. To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias is 10 V for each unit. The TLP-measured I-V characteristic of the LVPMOSs are shown in Fig. 2.8. The drain breakdown voltage of the LVPMOS unit is 10.5 V, and the trigger voltage (V_{t1}) is 10.41 V. LVPMOS can also be stacked up for higher trigger and holding voltage without losing I_{t2}. Although the ESD robustness is high, the holding voltage lower than the target supply voltage 10 V. It is possible that latchup occurs in applications.

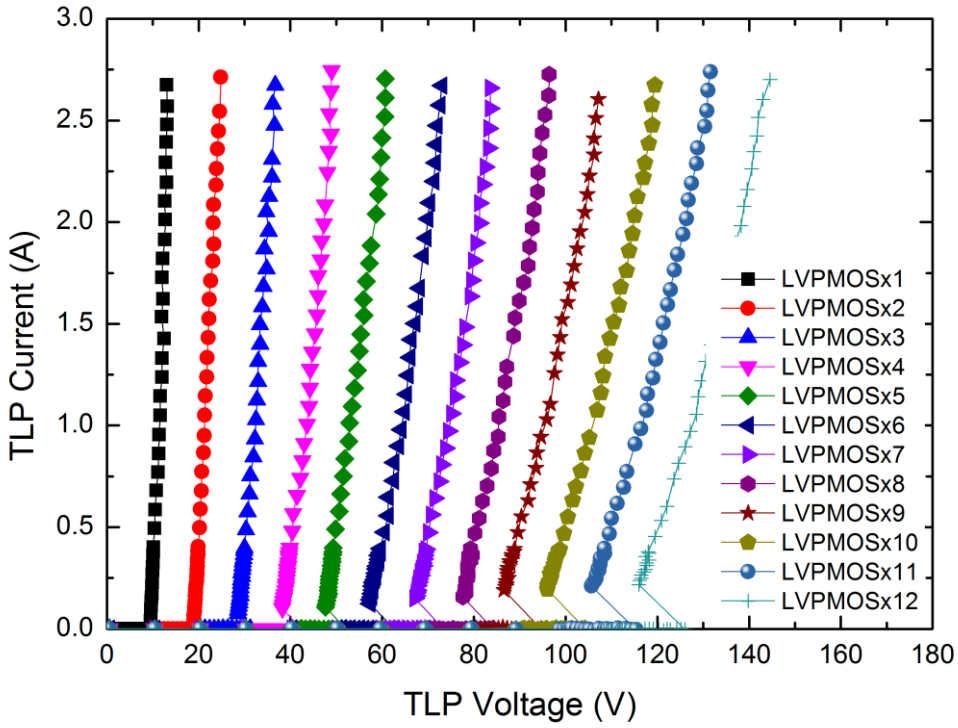


Fig. 2.8 Stacked LVPMOS TLP I-V curve characteristic.

The detailed characteristic of stacked LVPMOS with different stacking numbers are listed in TABLE 2.3. By adjusting the stacking numbers, all the parameters can linearly increase that proposed ESD protection solution can be further used for higher voltage applications. The LVPMOS has non-snapback phenomenon, which makes the curve to fit into the ESD protection window. But for the concern of latchup-free immunity, LVPMOS is not a choice for ESD protection. Or 13-LVPMOS stacked can be fit into the ESD protection window. LVPMOS has large leakage current when the applied voltage close to breakdown.

TABLE 2.3

Summary of Stacked LVPMOS TLP ESD Robustness with Different Stacking Numbers.

Stacked Number of LVPMOS	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*
1	10.41	9.55	2.57	10.5	5
2	20.33	19.01	2.54	20.5	5
3	31.22	28.56	2.58	31.0	5
4	42.29	38.23	2.53	41.5	5
5	52.05	47.68	2.61	52.0	5
6	62.60	57.34	2.57	61.5	5
7	73.40	67.16	2.56	72.0	5
8	84.11	77.58	2.62	82.0	5
9	94.62	86.57	2.51	92.5	5
10	104.22	96.03	2.58	104.0	5
11	115.37	105.65	2.65	113.0	5
12	126.04	115.96	2.60	123.5	5

(*) ESD failure criteria : BV (I @1μA) shift >20%.

For LVPFOD, the device dimension was drawn as W = 800 μm and S = 0.9 μm. To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias is 10 V for each unit. The TLP-measured I-V characteristic of the LVPFODs are shown in Fig. 2.9. The drain breakdown voltage of the LVPFOD unit is 11.0 V, and the trigger voltage (V_{t1}) is 12.52 V. LVPFOD can also be stacked up for higher trigger and holding voltage without losing I_{t2}. The LVPFOD unit can pass HBM ESD test of 4.5kV. And the holding voltage can higher than the target supply voltage 10 V. It is a good solution design, which is proposed to latchup-free immunity.

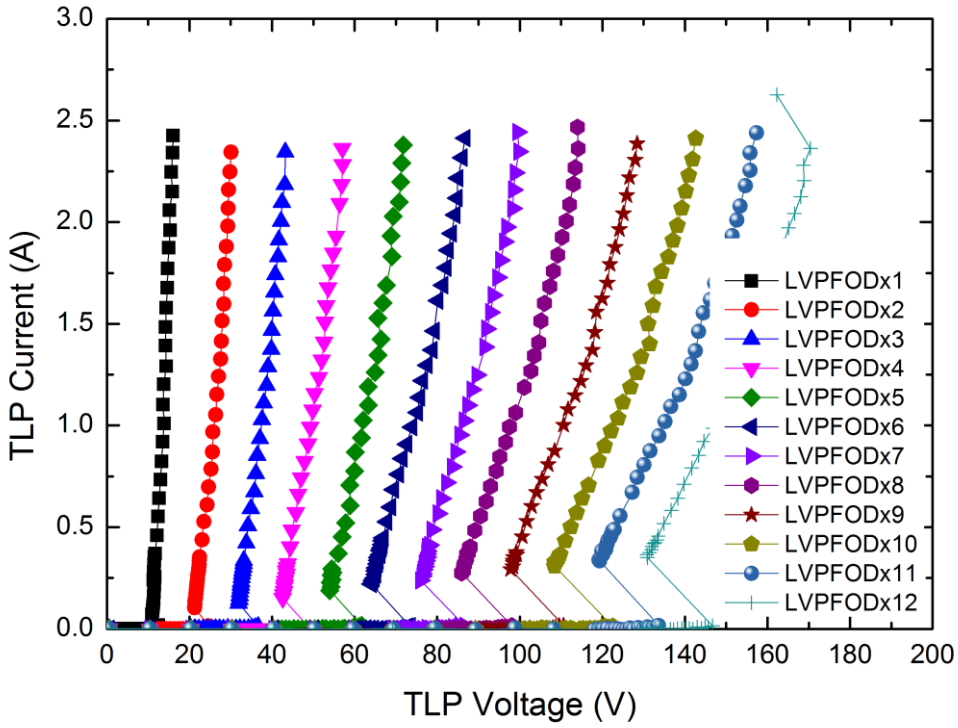


Fig. 2.9 Stacked LVPFOD TLP I-V curve characteristic.

The detailed characteristic of stacked LVPFOD with different stacking numbers are listed in TABLE 2.4. By adjusting the stacking numbers, all the parameters can linearly increase that proposed ESD protection solution can be further used for higher voltage applications and also get latchup-free immunity. The LVPFOD has non-snapback phenomenon, which makes the curve to fit into the ESD protection window. Stacked LVPFOD can be completed by less masks in process. And it is an excellent solution for latchup-free immunity and ESD robustness. An effective ESD protection solution realized with 12-LVPFOD stacked has been successfully verified in a 0.5-μm SOI process for 120 V applications.

TABLE 2.4

Summary of Stacked LVPFOD TLP ESD Robustness with Different Stacking Numbers.

Stacked Number of LVPFOD	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*
1	12.52	10.91	2.34	11.0	4.5
2	24.67	21.25	2.25	22.5	4.5
3	36.66	31.94	2.19	34.0	4.5
4	48.78	42.56	2.28	45.5	4.5
5	61.71	54.00	2.29	56.5	4.5
6	73.52	64.08	2.32	68.0	4.5
7	86.69	76.31	2.35	79.0	4.5
8	98.06	85.93	2.36	90.5	4.5
9	110.57	97.83	2.30	101.5	4.5
10	122.52	108.42	2.31	113.0	4.5
11	133.69	119.22	2.34	124.5	4.5
12	146.71	130.82	2.36	135.5	4.5

(*) ESD failure criteria : BV (I @1μA) shift >20%.

As shown in Fig. 2.10, it depicts the comparison among three DC I-V curves of LV ESD protection devices in SOI process. The DC I-V curve of LVPMOS is larger than the others at 10 V. LVPMOS has large leakage current when the applied voltage close to breakdown. With consideration for ESD robustness, LVPFOD can be the best choice of stacked configuration.

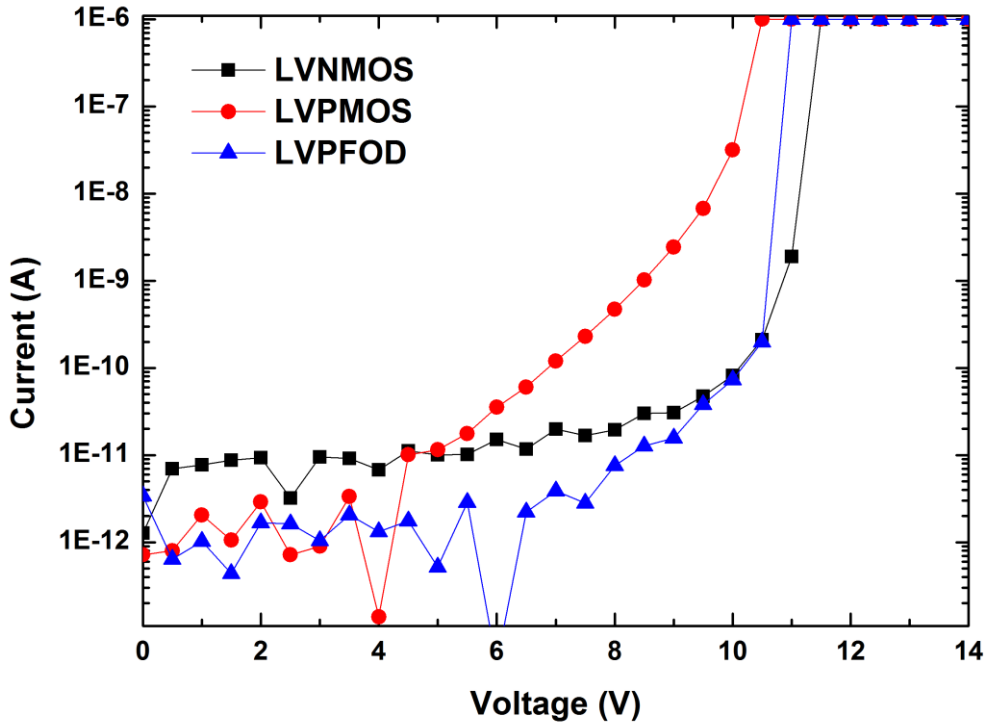


Fig. 2.10 DC measurement of LV ESD protection devices.

2.5 Summary

This chapter focuses on ESD protection design for 120 V application in high-voltage ICs. Each unit device was fully isolated to each other by the DTI and buried oxide. 12-LVPFOD stacked structure has been successfully verified in a 0.5-μm SOI process for 120 V applications. Every LVPFOD was only connected through the metal layers to make the stacked configuration with different stacking numbers. The TLP-measured I-V characteristic of the 12-LVPFOD stacked is shown in Fig. 2.9. The detailed characteristic of 12-stacked

LVPFOD is listed in TABLE 2.4. LVPFOD without gate structure does not suffer the leakage problem. LVPMOS has large leakage current when the applied voltage close to breakdown. LVNMOS burned out immediately when entering into its snapback region.

The trigger voltage (Vt1, 146.7 V) of stacked 12-LVPFOD can be smaller than the breakdown voltage (147.0 V) of 120 V nLDMOS to get an effective ESD protection. The holding voltage (Vh, 130.82 V) of stacked LVPFOD can be greater than the maximum operation voltage (Vcc, 120 V) to avoid latchup issue. The 12-LVPFOD stacked also exhibited excellent ESD robustness of up to 4.5 kV in HBM ESD test. TABLE 2.5 depicts the comparison among HV ESD protection in SOI process with the previous arts. The silicon data shows that stacked LVPFOD applied for 120V application in SOI process can pass 4kV HBM level with reasonable layout area.

TABLE 2.5

Comparison of HV ESD Protection Solutions among the Prior Arts in SOI Process.

ESD solutions	Technology (SOI)	Device used for ESD protection	Supply voltage (Vcc)	TLP (100ns)			HBM ESD level	Device width (μm)	Latchup issue (*2)
				V_{t1} (V)	V_h (V)	I_{t2} (A)			
[4]	40V SOI LDMOS process	LDMOS-SCR	40V	53	4	1.25	N.A.	N.A.	Yes
[5]	60V SOI BCD process	LDMOS-SCR	60V	70	3.5	1.25	N.A.	N.A.	Yes
[6]	0.18μm 60V SOI BCD process	LDMOS-SCR	60V	65	10	2.5	N.A.	40	Yes
[7], [8]	0.8μm SOI BCD process	LDMOS-SCR	25V	37	3	5.5	N.A.	300	Yes
[9]	SOI process	LDMOS-SCR	42V	65	5	>10	N.A.	N.A.	Yes
[10]	0.5μm SOI process	LDMOS-SCR	15V	42	17	5.1	N.A.	120	No
[11]	0.18μm 40V SOI BCD process	LDMOS	40V	47	10	2.14	N.A.	N.A.	Yes
This work	0.5μm 120V SOI process	12-LVPFOD stacked	120V	146.7	130.9	2.36	4.5kV (*1)	800	No

(*1) ESD failure criteria : BV (I @1μA) shift >20%.

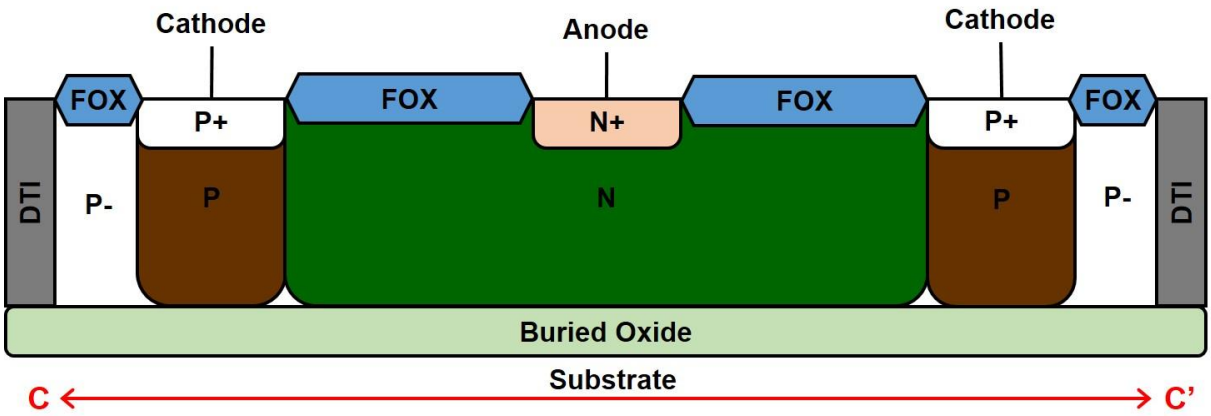
(*2) The holding voltage (V_h) should be larger than the supply voltage (V_{CC}) to avoid latchup issue.

Chapter 3

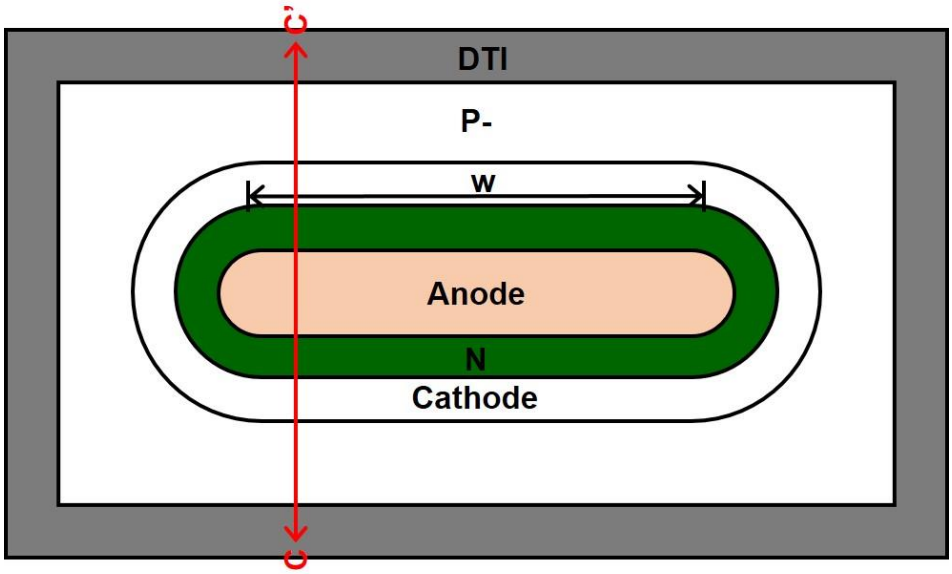
Stacked Low-Voltage and High-Voltage Devices

3.1 High-Voltage Device Structures

In this chapter, the proposed solution will use the stacked LV-HV Device Structures. The simplified device cross-sectional view and the corresponding layout top view of the HV-Diodes are shown in Fig. 3.1 (a) and 3.1 (b), respectively. In SOI process, HV device structures are made like racetrack type. For 60 V and 80 V high-voltage applications, the difference between two voltage applications is design rule in the same structure. The width is defined by the straight line among racetrack type structure. The HBM ESD target levels of HV-Diode in the testchip are 2 kV, 4 kV, and 8 kV. The device dimensions were drawn as total W of 3000 μm, 5000 μm, and 9000 μm, respectively. They were fully isolated by the DTI and buried oxide. The typical devices of HV-Diode had been drown with minimum rule of the given SOI process. In reverse bias region, to breakdown the junction has large enough voltage across the device. As an ESD protection devices, it would not snapback, which means the holding voltage is higher than the supply voltage. It can be an excellent solution for latchup-free immunity.



(a)



(b)

Fig. 3.1 Device (a) cross-sectional view, and (b) layout top view of HV-Diode in a 0.5-μm SOI process.

3.2 Low-Voltage and High-Voltage Device Characteristics

3.2.1 Low-Voltage Devices

The HBM ESD target levels of LVPFOD in the testchip are 2 kV, 4 kV, and 8 kV. The device dimensions were drawn as total W of 600 μm, 800 μm, and 1600 μm, respectively. They were fully isolated by the DTI and buried oxide. The typical devices of LVPFOD had been drown with minimum rule of the given SOI process. To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias is 10 V. The TLP-measured I-V characteristic of the LVPFOD with different width are shown in Fig. 3.2. The drain breakdown voltage of the LVPFOD with different width are the same voltage 11.0 V. And the trigger voltage (V_{t1}) are 12.40 V, 12.34 V, and 12.21 V, respectively. And the holding voltage can higher than the target supply voltage 10 V. It not only proposed to latchup-free immunity but also accomplished the HBM ESD target levels.

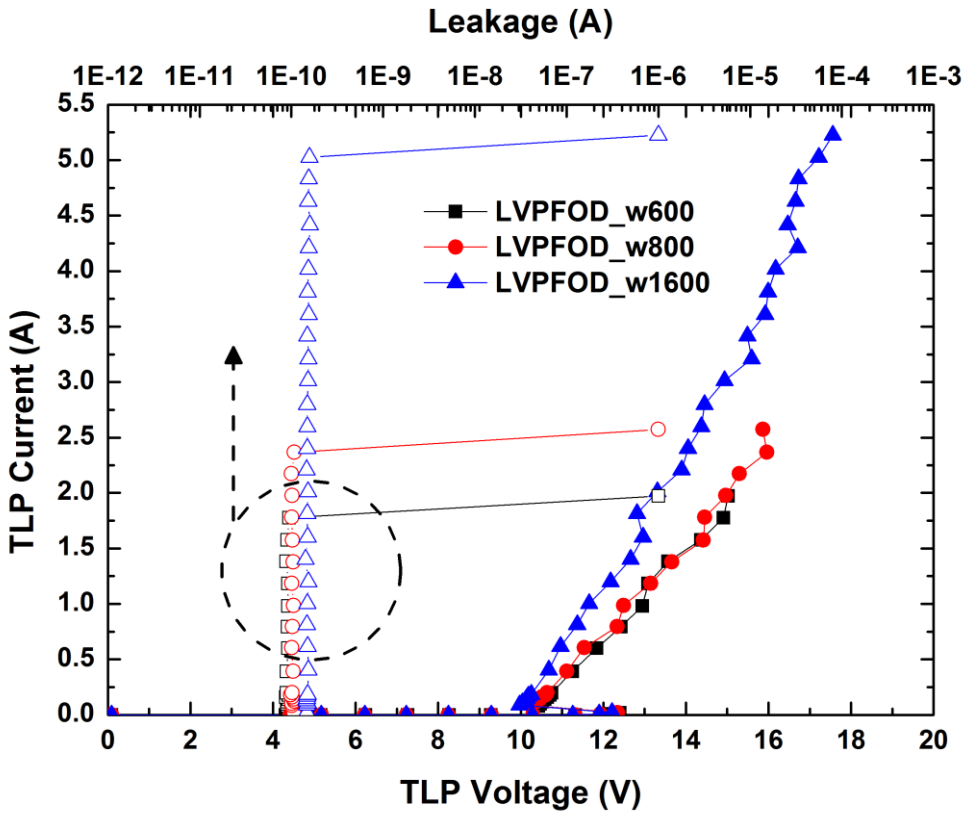


Fig. 3.2 LVPFOD TLP I-V curve characteristic with different width.

The detailed characteristic of LVPFOD with different width are listed in TABLE 3.1. By adjusting the total width, the HBM ESD level can linearly increase that proposed ESD protection solution can be further used for higher ESD robustness. The LVPFOD has non-snapback phenomenon, which makes the curve to fit into the ESD protection window. Stacked LVPFOD can be completed by less masks in process. And it is an excellent solution for latchup-free immunity and ESD robustness.

TABLE 3.1

Summary of LVPFOD TLP ESD Robustness with Different Width.

LVPFOD width	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*	MM (V)*
600 μm	12.40	10.43	1.78	11.0	3.5	150
800 μm	12.34	10.25	2.37	11.0	4.5	250
1600 μm	12.21	9.97	5.02	11.0	>8	450

(*) ESD failure criteria : BV (I @1μA) shift >20%.

3.2.2 High-Voltage Devices

According to the chapter 3.1, the TLP-measured I-V characteristic of the 60 V and 80 V HV-Diode are shown in Fig. 3.3 and 3.4, respectively. To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias are 60 V for 60 V HV-Diode and 80 V for 80 V HV-Diode, respectively. The drain breakdown voltage of the 60 V HV-Diode is 91.0 V and the 80 V HV-Diode is 122.5 V. And the holding voltage can higher than the target supply voltage 60 V and 80 V, respectively. HV-Diode can also be increased up for higher I_{t2} without losing trigger and holding voltage. But the 80 V HV-Diode got bad ESD robustness, it cannot be an ESD protection devices.

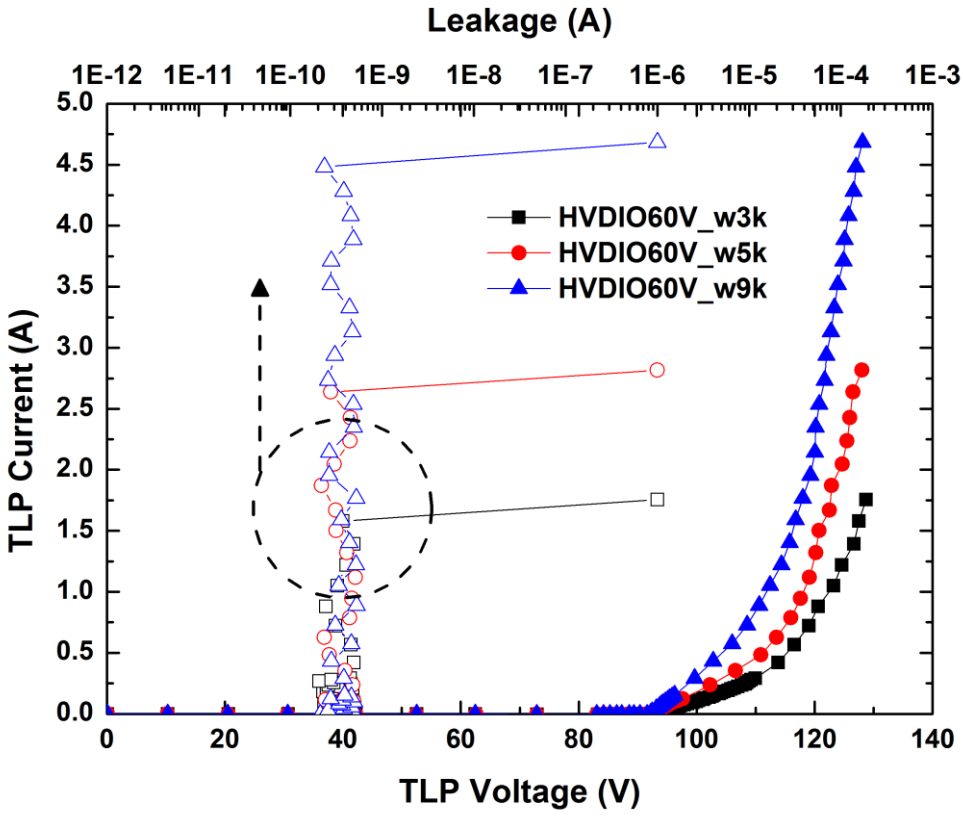


Fig. 3.3 60 V HV-Diode TLP I-V curve characteristic with different width.

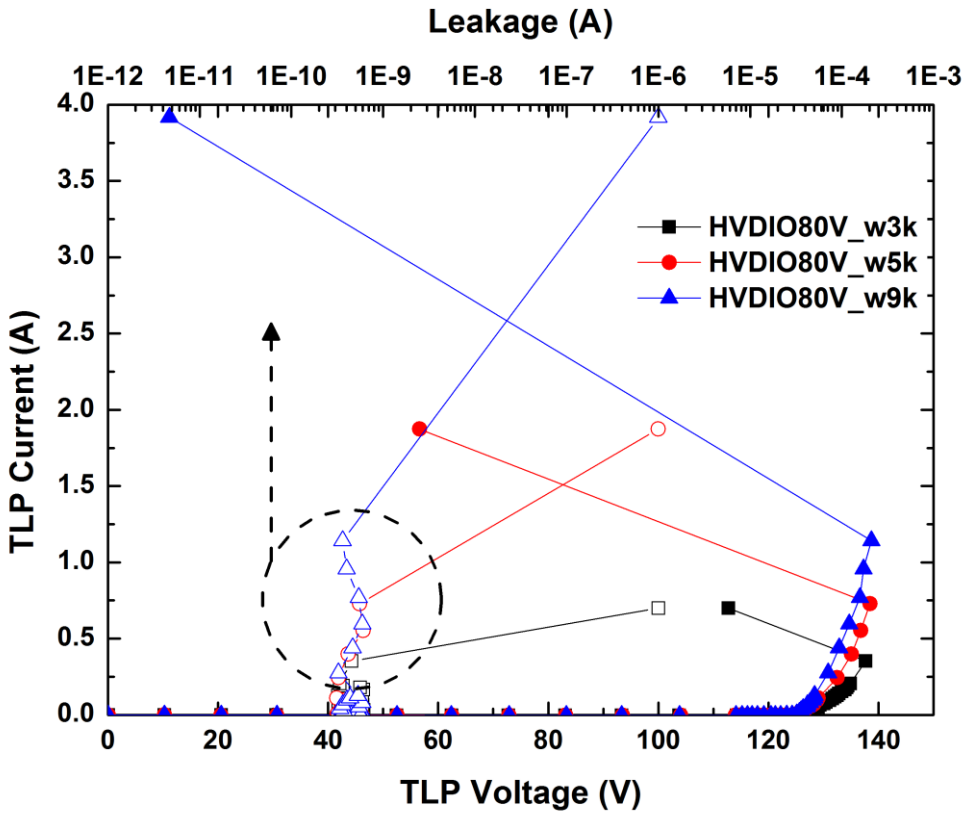


Fig. 3.4 80 V HV-Diode TLP I-V curve characteristic with different width.

The detailed characteristic of HV-Diodes with different width are listed in TABLE 3.2. By adjusting the total width, the HBM ESD level can linearly increase that proposed ESD protection solution can be further used for higher ESD robustness. The HV-Diode has non-snapback phenomenon, which makes the curve to fit into the ESD protection window. Even 60 V HV-Diode can accomplish the HBM ESD target levels, it is completed by more masks in process. For area and ESD concerns, ESD robustness per area of 60 V HV-Diode is smaller than LV device, not to mention the 80 V HV-Diode. The anode to cathode spacing of 60 V HV-Diode and 80 V HV-Diode are 7.99 μm and 9.19 μm, respectively. The turned-on central fingers cause the ESD current mainly discharging through those fingers. If the turned-on region cannot be extended to full regions of all fingers before second breakdown occurs in HV-Diodes, the turned-on central region will be burned out by the over-heating ESD current. It has a significant impact on 80 V HV-Diode.

TABLE 3.2

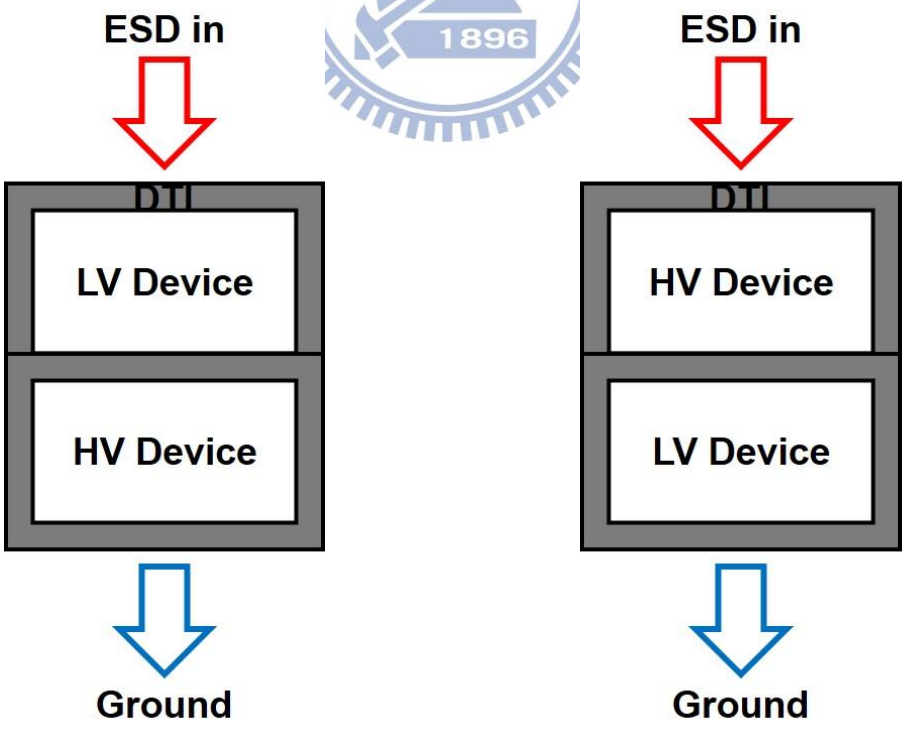
Summary of 60 V and 80 V HV-Diode TLP ESD Robustness with Different Width.

HV Diode operation voltage	HV Diode width	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*	MM (V)*
60 V	3000 μm	92.97	93.63	1.58	91.5	3	250
	5000 μm	91.93	92.73	2.64	91.0	5.5	400
	9000 μm	92.20	92.47	4.48	91.0	>8	550
80 V	3000 μm	125.12	125.95	0.35	122.0	0.5	200
	5000 μm	124.95	125.56	0.73	122.5	1.5	150
	9000 μm	125.15	125.58	1.14	122.5	2	150

(*) ESD failure criteria : BV (I @1μA) shift >20%.

3.2.3 Stacked Configurations

There are two stacked configurations, which are studied in this section. The top views of stacked configurations are shown in Fig. 3.5.



(a) (b)

Fig. 3.5 Top views of (a) stacked LV-HV, and (b) stacked HV-LV configuration.

All of these two stacked configurations are stacked by one LVPFOD (W = 600 μm) and one 60 V HV-Diode (W = 3000 μm). The TLP-measured I-V characteristic of stacked configurations are shown in Fig. 3.6. To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias is 70 V. The drain breakdown voltage of stacked LV-HV configuration is 106.5 V, and stacked HV-LV configuration is 110.0 V. And the trigger voltages (Vt1) are 110.18 V and 118.65 V, respectively. These two configurations can also be stacked up for higher trigger and holding voltage without losing I_{t2}.

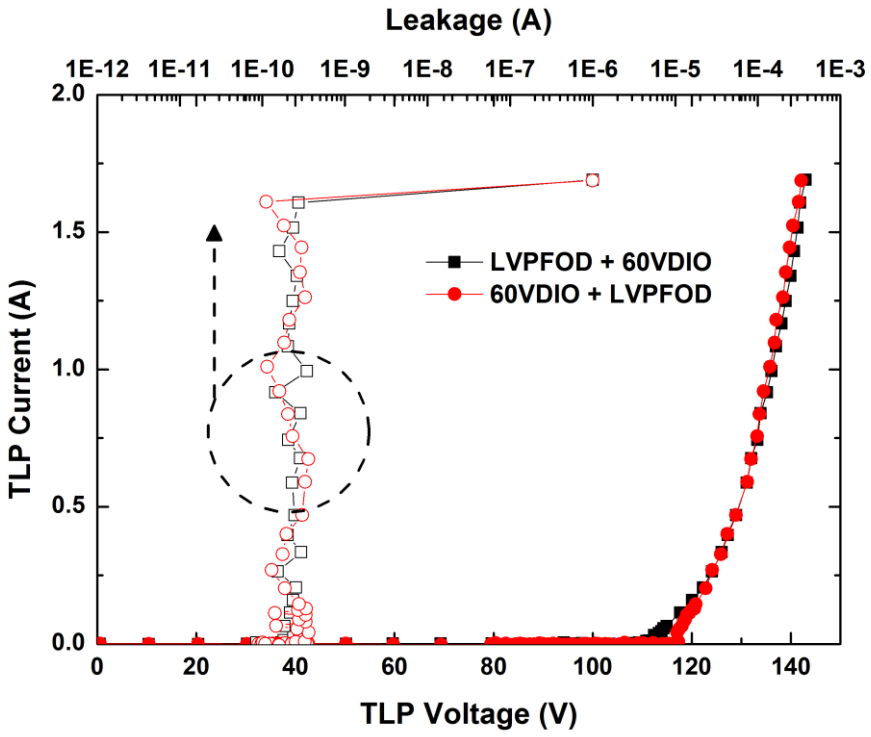


Fig. 3.6 Stacked configuration TLP I-V curve characteristic.

The detailed characteristic of stacked configurations are listed in TABLE 3.3. Stacked devices perform almost the same TLP I-V curves in LV-HV and HV-LV configuration. To choose the LV device for the first part of stacked configuration. Because of the stand-alone LV device got high HBM ESD level, so the HBM ESD level of stacked configuration is limited by HV device. For the reason that the best choice of stacked configuration is stacked LV-HV configuration.

TABLE 3.3

Summary of Stacked Configuration TLP ESD Robustness.

Stacked configuration	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*
LV-HV	110.18	110.82	1.61	106.5	3.5
HV-LV	118.65	119.02	1.61	110.0	3

(*) ESD failure criteria : BV (I @1μA) shift >20%.

3.3 Stacked Device Characteristics

3.3.1 For 120 V Application

In this section, there are three stacked methods for 120 V application listed below. (1) Two LVPFOD and one 80 V HV-Diode (2) Four LVPFOD and one 60 V HV-Diode (3) 12-LVPFOD stacked

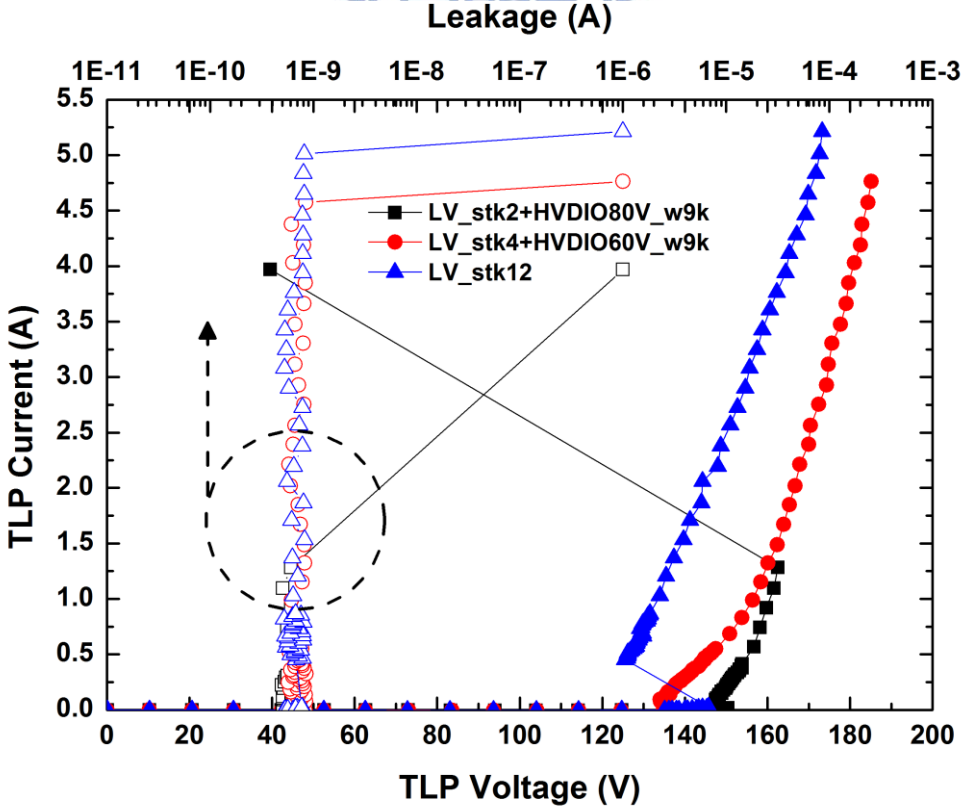


Fig. 3.7 For 120 V application TLP I-V curve characteristic.

To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias is 120 V. The TLP-measured I-V characteristic of the 120 V application are shown in Fig. 3.7. The drain breakdown voltage of the stacked methods for 120 V application are 142.5 V, 132.5 V, and 132.5 V, respectively. And the trigger voltage (V_{t1}) are 148.93 V, 143.79 V, and 145.69 V, respectively.

The detailed characteristic of stacked devices with different width for 120 V application are listed in TABLE 3.4. By adjusting the total width, the HBM ESD level can linearly increase that proposed ESD protection solution can be further used for higher ESD robustness. All the stacked methods have non-snapback phenomenon, which make the curve to fit into the ESD protection window. Obviously, 12-LVPFOD stacked is an excellent solution for latchup-free immunity and ESD robustness. It can be completed by less masks in process.

TABLE 3.4

Summary of Stacked Devices TLP ESD Robustness for 120 V Application.

For 120 V application	Device width (μm)	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*	MM (V)*	Area (μm^2)
LVPFOD x2+ 80V HV-Diode	LV:600 HV:3000	150.49	149.62	0.47	143.0	1	200	59167
	LV:800 HV:5000	150.23	149.17	0.85	142.5	1.5	150	94191
	LV:1600 HV:9000	148.93	148.88	1.28	142.5	2.5	150	157837
LVPFOD x4+ 60V HV-Diode	LV:600 HV:3000	142.59	140.32	1.55	134.0	3	350	52724
	LV:800 HV:5000	141.49	137.93	2.38	133.5	5	350	79960
	LV:1600 HV:9000	143.79	143.75	4.57	132.5	>8	600	134927
LVPFOD x12	LV:600	148.19	131.78	1.82	133.0	3.5	350	49152
	LV:800	146.96	129.53	2.42	135.5	5	400	60170
	LV:1600	145.69	125.55	5.01	132.5	>8	650	100960

(*) ESD failure criteria : BV (I @1μA) shift >20%.

3.3.2 For 150 V Application

In this section, there are five stacked methods for 150 V application listed below. (1) two 60 V HV-Diode (2) five LVPFOD and one 80 V HV-Diode (3) seven LVPFOD and one 60 V HV-Diode (4) 15-LVPFOD stacked (5) 16-LVPFOD stacked

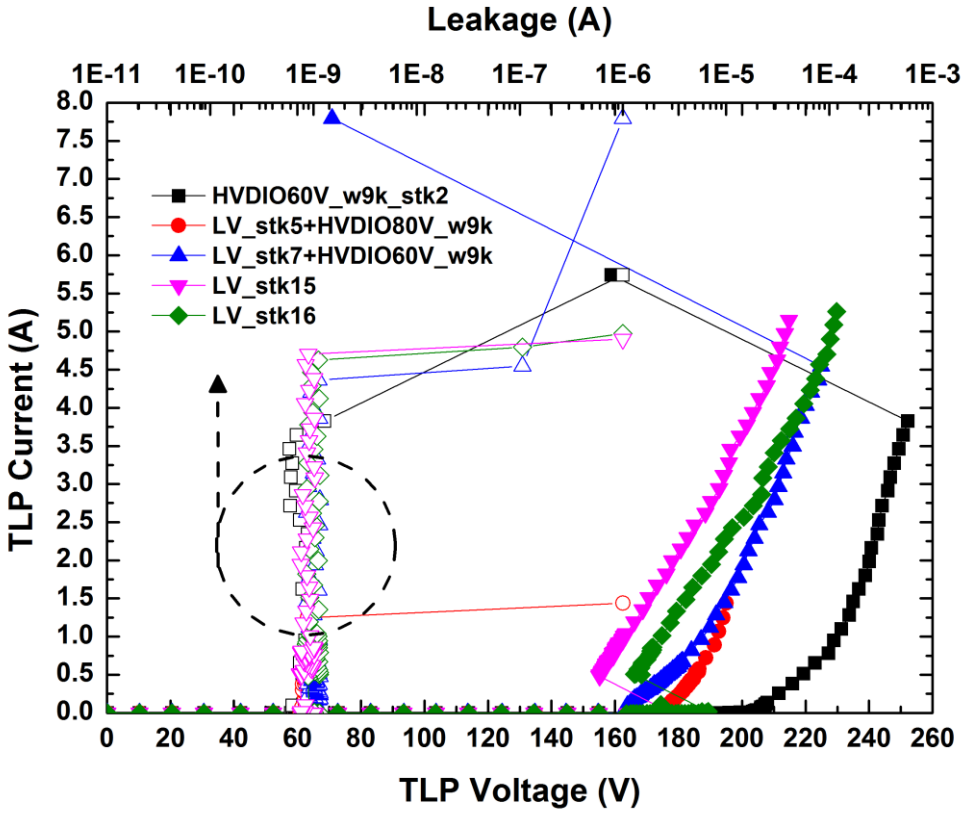


Fig. 3.8 For 150 V application TLP I-V curve characteristic.

To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias is 150 V. The TLP-measured I-V characteristic of the 150 V application are shown in Fig. 3.8. The drain breakdown voltage of the stacked methods for 150 V application are 183.5 V, 175.5 V, 166.3 V, 165.1 V, and 176.3 V, respectively. And the trigger voltages (V_{t1}) are 201.97 V, 181.53 V, 172.54 V, 177.36 V, and 186.27 V, respectively.

The detailed characteristic of stacked devices with different width for 150 V application are listed in TABLE 3.5. By adjusting the total width, the HBM ESD level can linearly increase that proposed ESD protection solution can be further used for higher ESD robustness. All the stacked methods have non-snapback phenomenon, which make the curve to fit into the

ESD protection window. The methods (3) seven LVPFOD and one 60 V HV-Diode, (4) 15-LVPFOD stacked, and (5) 16-LVPFOD stacked can accomplish the HBM ESD target levels. For area and ESD robustness concerns, LVPFOD is proved with good ESD robustness per area. Obviously, 15-LVPFOD stacked is an excellent solution for latchup-free immunity and ESD robustness.

TABLE 3.5

Summary of Stacked Devices TLP ESD Robustness for 150 V Application.

For 150 V application	Device width (μm)	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*	MM (V)*	Area (μm^2)
60V HV-Diode x2	HV:3000	205.92	207.24	1.36	184.3	2	400	71932
	HV:5000	204.71	205.39	2.38	184.3	3.5	450	118836
	HV:9000	201.97	202.80	3.83	183.5	6	650	201250
LVPFOD x5+ 80V HV-Diode	LV:600 HV:3000	186.91	182.83	0.42	176.7	1	250	59313
	LV:800 HV:5000	183.09	179.70	0.79	176.3	1.5	150	94381
	LV:1600 HV:9000	181.53	181.43	1.25	175.5	2.5	200	158375
LVPFOD x7+ 60V HV-Diode	LV:600 HV:3000	177.15	172.92	1.57	169.5	3	400	68803
	LV:800 HV:5000	171.01	167.09	2.36	169.9	5	400	99644
	LV:1600 HV:9000	172.54	172.32	4.55	166.3	>8	600	168139
LVPFOD x15	LV:600	182.21	164.98	1.82	166.3	3.5	400	61310
	LV:800	182.15	162.25	2.41	165.9	5	450	74997
	LV:1600	177.36	155.13	4.98	165.1	>8	700	125895
LVPFOD x16	LV:600	195.61	176.47	1.77	177.5	3.5	450	65231
	LV:800	194.65	173.28	2.51	177.1	5	500	79854
	LV:1600	186.27	174.44	5.09	176.3	>8	750	134173

(*) ESD failure criteria : BV (I @1μA) shift >20%.

3.3.3 For 200 V Application

In this section, there are five stacked methods for 200 V application listed below. (1) two 80 V HV-Diode (2) ten LVPFOD and one 80 V HV-Diode (3) four LVPFOD and two 60 V HV-Diode (4) 20-LVPFOD stacked (5) 21-LVPFOD stacked

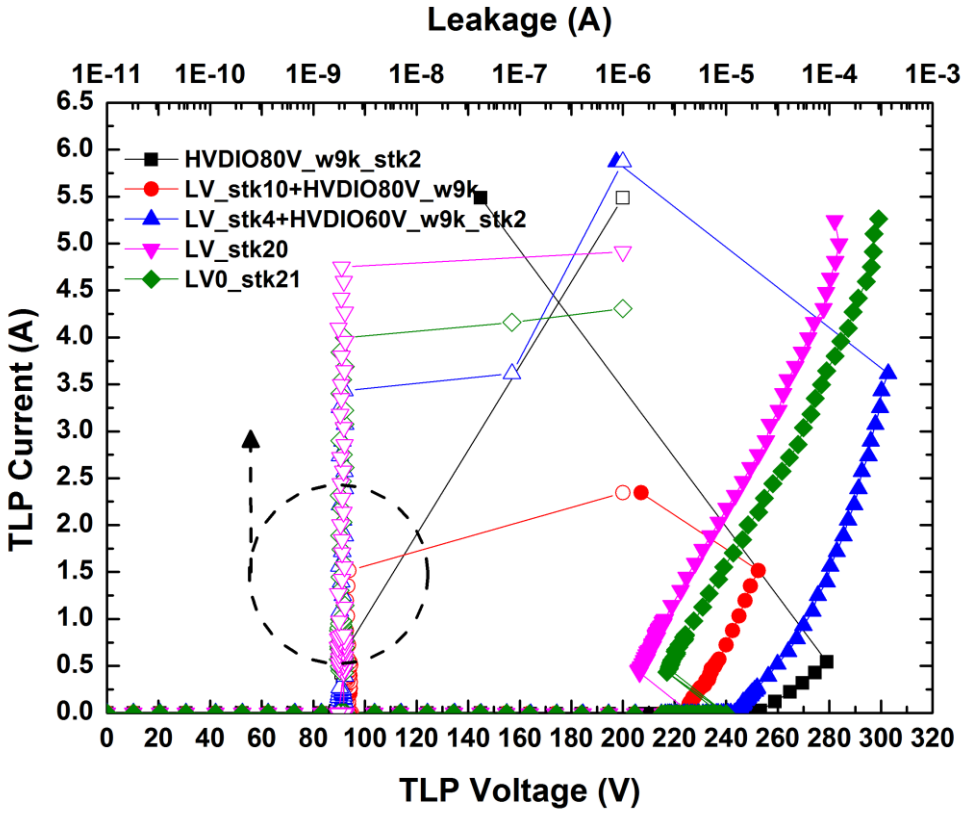


Fig. 3.9 For 200 V application TLP I-V curve characteristic.

To measure the TLP I-V curve, the failure criteria is determined by the leakage current over 1 μA when the drain bias is 200 V. The TLP-measured I-V characteristic of the 200 V application are shown in Fig. 3.9. The drain breakdown voltage of the stacked methods for 200 V application are 209.5 V, 211.0 V, 217.0 V, 221.5 V, and 233.5 V, respectively. And the trigger voltages (V_{t1}) are 251.37 V, 228.20 V, 243.84 V, 226.67 V, and 239.99 V, respectively.

The detailed characteristic of stacked devices with different width for 200 V application are listed in TABLE 3.6. By adjusting the total width, the HBM ESD level can linearly increase that proposed ESD protection solution can be further used for higher ESD robustness. All the stacked methods have non-snapback phenomenon, which make the curve to fit into the

ESD protection window. The methods (4) 20-LVPFOD stacked and (5) 21-LVPFOD stacked can accomplish the HBM ESD target levels. For area and ESD robustness concerns, LVPFOD is proved with good ESD robustness per area. Obviously, 20-LVPFOD stacked is an excellent solution for latchup-free immunity and ESD robustness.

TABLE 3.6

Summary of Stacked Devices TLP ESD Robustness for 200 V Application.

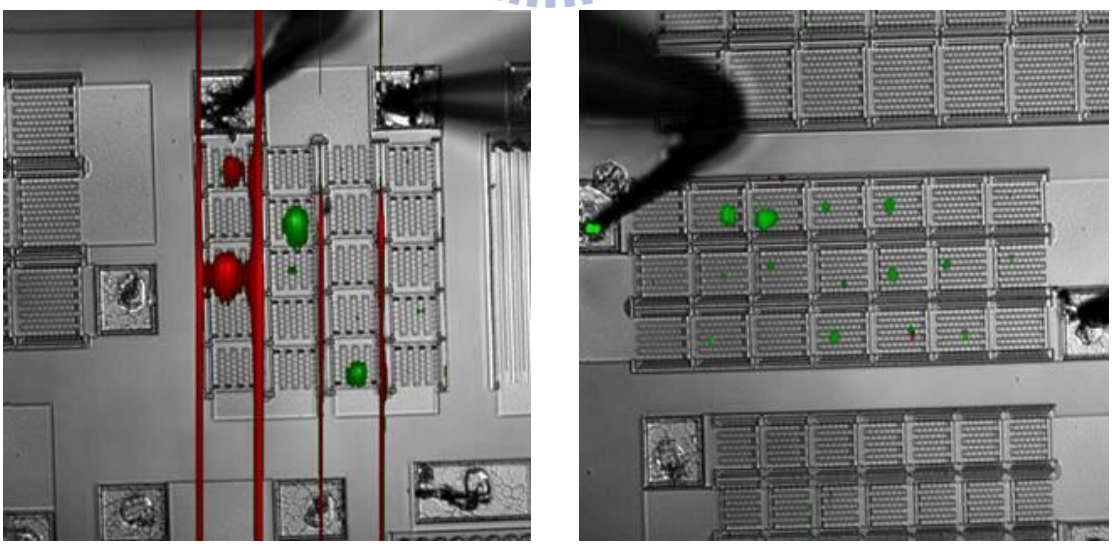
For 200 V application	Device width (μm)	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	HBM (kV)*	MM (V)*	Area (μm^2)
80V HV-Diode x2	HV:3000	252.27	253.13	0.16	211.0	0.5	250	77049
	HV:5000	251.82	251.76	0.33	209.5	1	250	137743
	HV:9000	251.37	251.33	0.54	209.5	1	250	231482
LVPFOD x10+ 80V HV-Diode	LV:600 HV:3000	242.42	236.36	0.39	214.0	<0.5	200	79341
	LV:800 HV:5000	234.35	230.59	0.86	212.5	1.5	150	118438
	LV:1600 HV:9000	228.20	226.24	1.52	211.0	2.5	150	199112
LVPFOD x4+ 60V HV-Diode x2	LV:600 HV:3000	251.18	250.43	1.35	220.0	2	450	87913
	LV:800 HV:5000	247.79	247.47	2.31	218.5	3.5	400	138421
	LV:1600 HV:9000	243.84	244.17	3.62	217.0	6	500	234322
LVPFOD x20	LV:600	243.89	222.16	1.71	223.0	3.5	500	81253
	LV:800	242.62	218.43	2.44	223.0	5	550	99832
	LV:1600	226.67	206.49	5.00	221.5	>8	800	167310
LVPFOD x21	LV:600	255.44	234.06	1.80	235.0	3.5	500	85370
	LV:800	252.08	229.01	2.38	233.5	5	600	104652
	LV:1600	239.99	217.87	5.10	233.5	>8	800	175765

(*) ESD failure criteria : BV (I @1μA) shift >20%.

3.4 Failure Analysis

In semiconductor Failure Analysis Optical Beam Induced Resistance Change (OBIRCH) is commonly used to locate a metal short or an active area short. OBIRCH is normally used for resistance variation analysis and current leak analysis inside the chip. Principle of the OBIRCH approach is an optical beam (IR) scans the IC and monitors the corresponding current at exact location. The beam induced heat inside the chip locally. Only near defects this heat generation will cause a local resistance change. This location is stored and can be overlapped an initial image produced by laser scanning the chip. The red point indicates high resistance and the green point indicates low resistance.

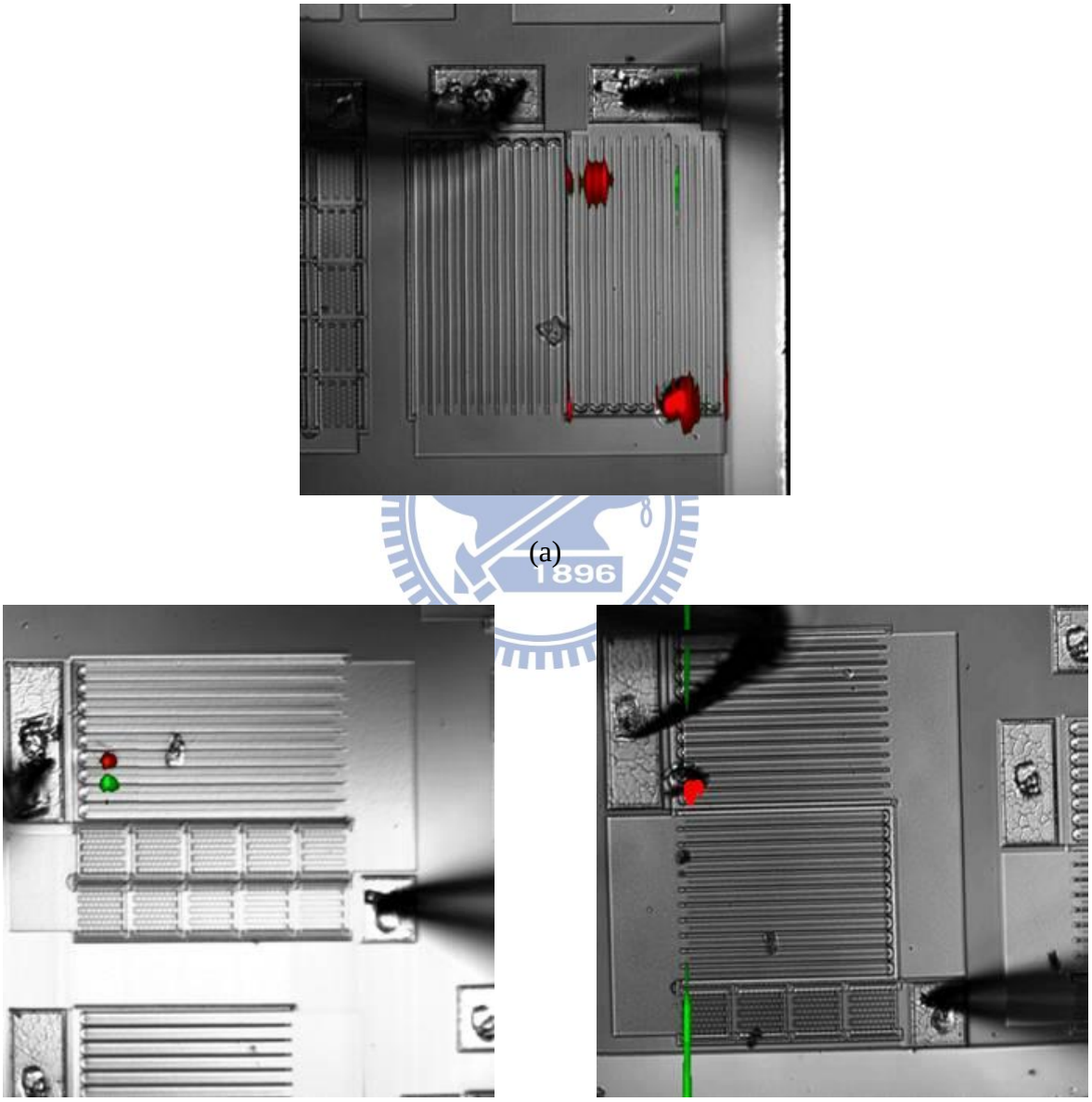
In condition of 200 V application, using OBRICH to prove the failure phenomenon. The current of stacked LVPFOD can be uniformly discharged through every stacked device, as shown in Fig 3.10. The defects are caused some local resistance change uniformly. The failure locations of the device fingers have ESD damage in the images. And HBM ESD level does not decrease with different stacking numbers. So stacked LVOFOD is an excellent solution for ESD protection device.



(a) (b)

Fig. 3.10 OBRICH image of (a) 20-LVPFOD stacked, and (b) 21-LVPFOD stacked.

As shown in Fig. 3.11, the localized ESD damage of stacked HV device is only found within some region of one finger, due to the non-uniform turn-on phenomenon. The HBM ESD level of LVPFOD device is higher than HV-Diode. So the stacked LV-HV device HBM ESD level is limited by HV device. So stacked HV device is a poor solution for ESD protection device.



(a)

(b) (c)

Fig. 3.11 The OBRICH image of (a) two 80 V HV-Diode, (b) ten LVPFOD and one 80 V HV-Diode, and (c) four LVPFOD and two 60 V HV-Diode.

3.5 Summary

This chapter focuses on ESD protection design for 120 V, 150 V and 200 V operation voltages, in a 0.5-μm SOI process. Stacked LV-HV device structures have been successfully verified in a 0.5-μm SOI process. As ESD protection devices, HV-Diodes and LVPFOD have no snapback phenomenon, which can become excellent solutions for latchup-free ESD protection design. But LV devices have higher ESD robustness than HV devices with same area. The HBM ESD level of stacked configuration is limited by HV device. In 80 V HV-Diode, no matter how to modify the total width, the ESD robustness is still poor. 60 V HV-Diode is much better than 80 V HV-Diode, but HV-Diodes have lower ESD robustness than stacked LVPFOD with same area. With consideration for layout area and ESD robustness, stacked LVPFOD can be the best choice. The proposed ESD protection solution can be further used for higher voltage applications with latchup-free immunity.

Chapter 4

HBM and MM ESD Effect of Stacked Devices

4.1 Stacked Low-Voltage Device Characteristics

There is an investigation of MM ESD level in this chapter. The MM ESD level of the stacked LVPFOD with different stacking numbers is shown in Fig. 4.1. According to the chapter 2, HBM ESD level has same ESD level, it does not increase with the numbers of stacked devices. And it is different with HBM ESD level, the MM ESD level increases with the numbers of stacked devices. The MM ESD level is proportional to the stacked number.

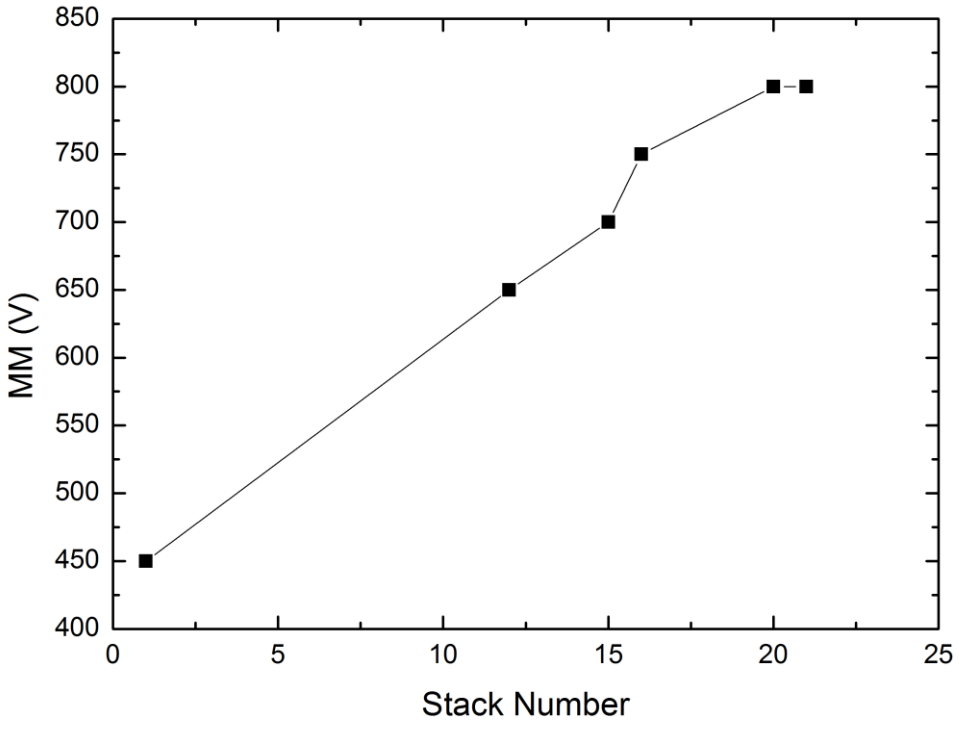


Fig. 4.1 MM ESD test level with different stacking numbers.

The TLP-measured I-V characteristic of the stacked LVPFOD with different stacking numbers are shown in Fig. 4.2. The trigger voltage (V_{t1}) of stacked LVPFOD can be smaller

than the breakdown voltage of HV LDMOS to get an effective ESD protection. The holding voltage (V_h) of stacked LVPFOD can be greater than the maximum operation voltage (Vcc) to avoid latchup issue.

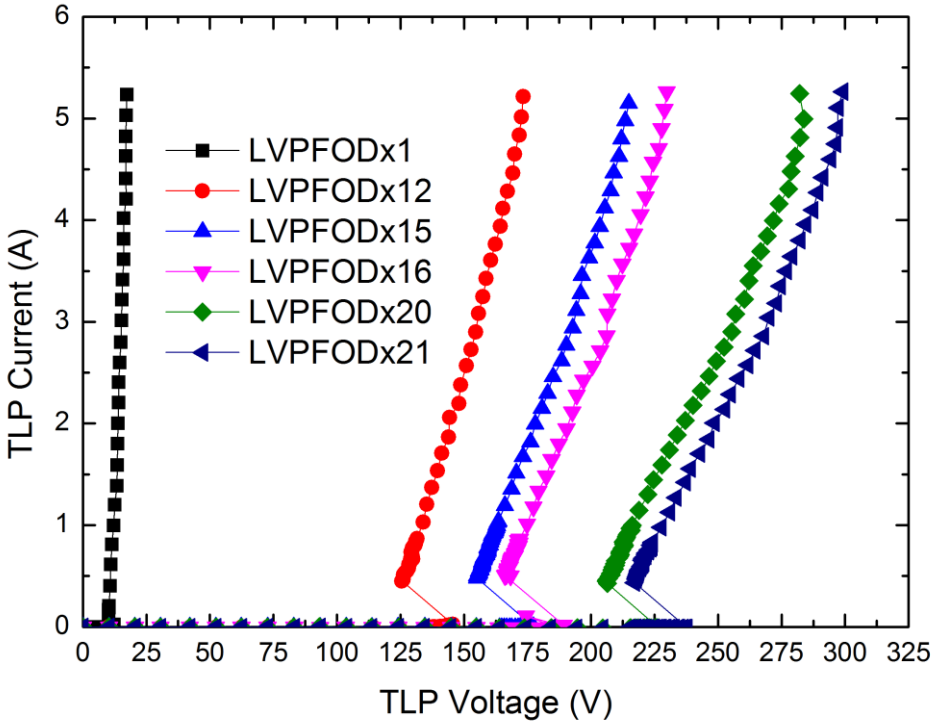


Fig. 4.2 TLP-measured I-V characteristic of the stacked LVPFOD with different stacking numbers of 1, 12, 15, 16, 20 ,and 21, verified in a 0.5-μm SOI process.

The trend of V_{t1} and V_h with different stacking numbers is shown in Fig. 4.3. They can linearly increase by the numbers of LVPFOD stacked. The on-state resistance (R_{on}) of stacked LVPFOD can also linearly increase by the numbers of LVPFOD stacked. The second breakdown current (It2) with different stacking numbers of stacked LVPFOD can achieve 5 A. It means the current can uniformly through the every unit device, and does not decrease with different stacking numbers. The trend of R_{on} and I_{t2} with different stacking numbers is shown in Fig. 4.4.

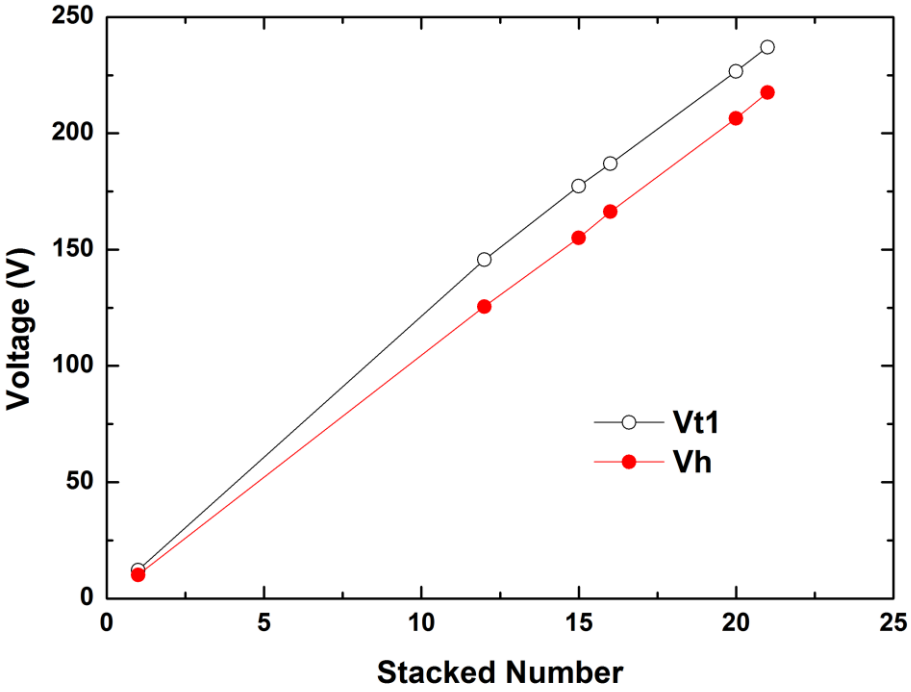


Fig. 4.3 TLP trigger voltage and holding voltage with different stacking numbers.

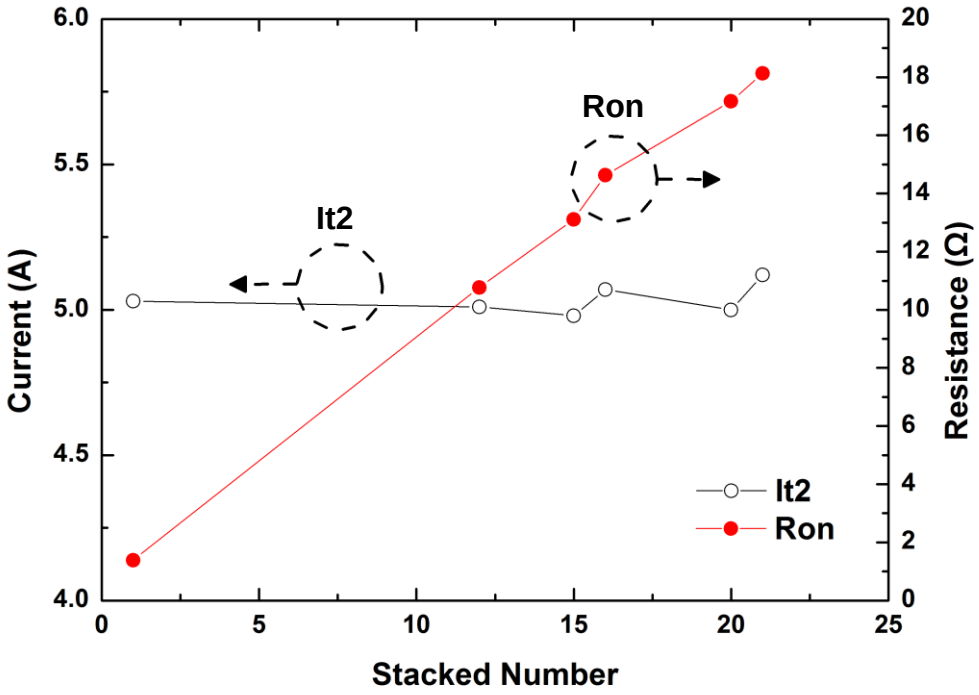


Fig. 4.4 TLP second breakdown current and on-state resistance with different stacking numbers.

The detailed characteristic of stacked LVPFOD with different stacking numbers are listed in TABLE 4.1. The silicon data shows that stacked LVPFOD applied for 120V application in a HV SOI process can pass 8kV HBM level with reasonable layout area. By adjusting the stacking numbers, all the parameters can linearly increase that proposed ESD protection solution can be further used for higher voltage applications and also get latchup-free immunity.

TABLE 4.1

Summary of Stacked LVPFOD TLP ESD Robustness with Different Stacking Numbers.

Stacked Number of LVPFOD	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V) (I@1μA)	R_{on} (Ω)	HBM (kV)*	MM (V)*
1	12.20	10.14	5.03	11.0	1.39	>8	450
12	145.69	125.55	5.01	132.5	10.77	>8	650
15	177.36	155.13	4.98	165.1	13.11	>8	700
16	186.93	166.30	5.07	176.3	14.63	>8	750
20	226.67	206.49	5.00	221.5	17.17	>8	800
21	237.04	217.48	5.12	233.5	18.13	>8	800

(*) ESD failure criteria : BV (I @1μA) shift >20%.

4.2 Current Waveform Measurement

4.2.1 Measurement setup

As shown in TABLE 4.1, all the HBM ESD level are the same, but the MM ESD level increases by the numbers of stacked LVPFOD. Because of the device resistance increases by the numbers of stacked LVPFOD. Base on JEDEC standards [13], [14], methods with peak current (Ipeak) test had been defined. The typical equivalent HBM and MM ESD test circuits are shown in Fig. 4.5 and 4.6, respectively.

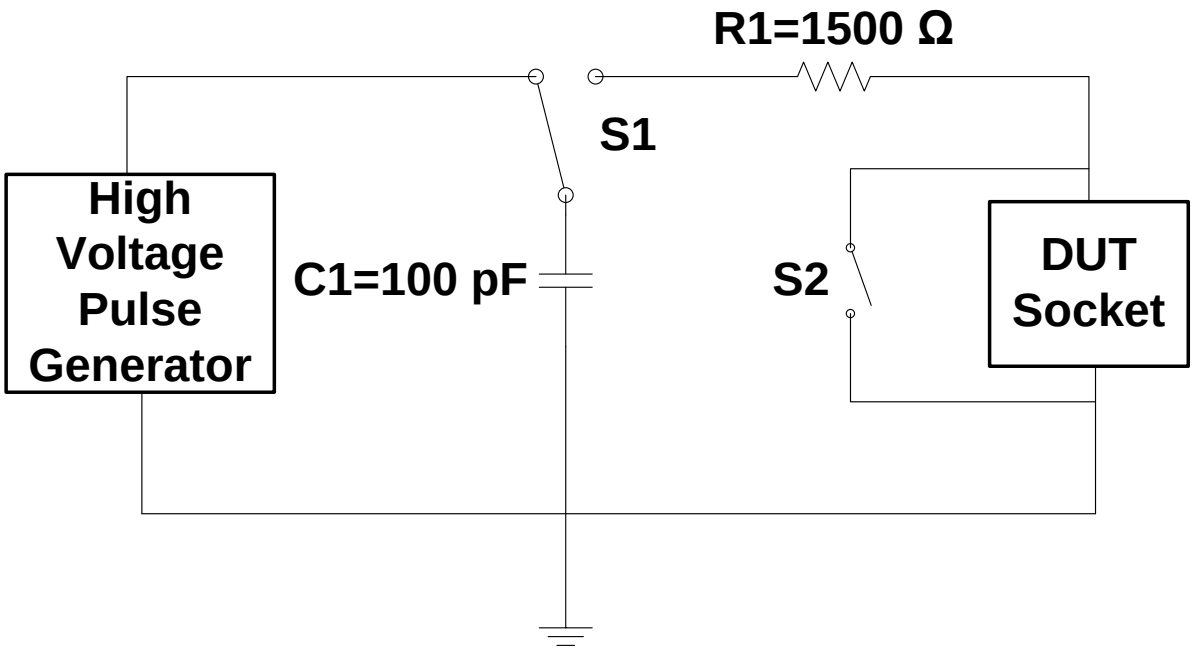


Fig. 4.5 Typical equivalent HBM ESD circuit [13].

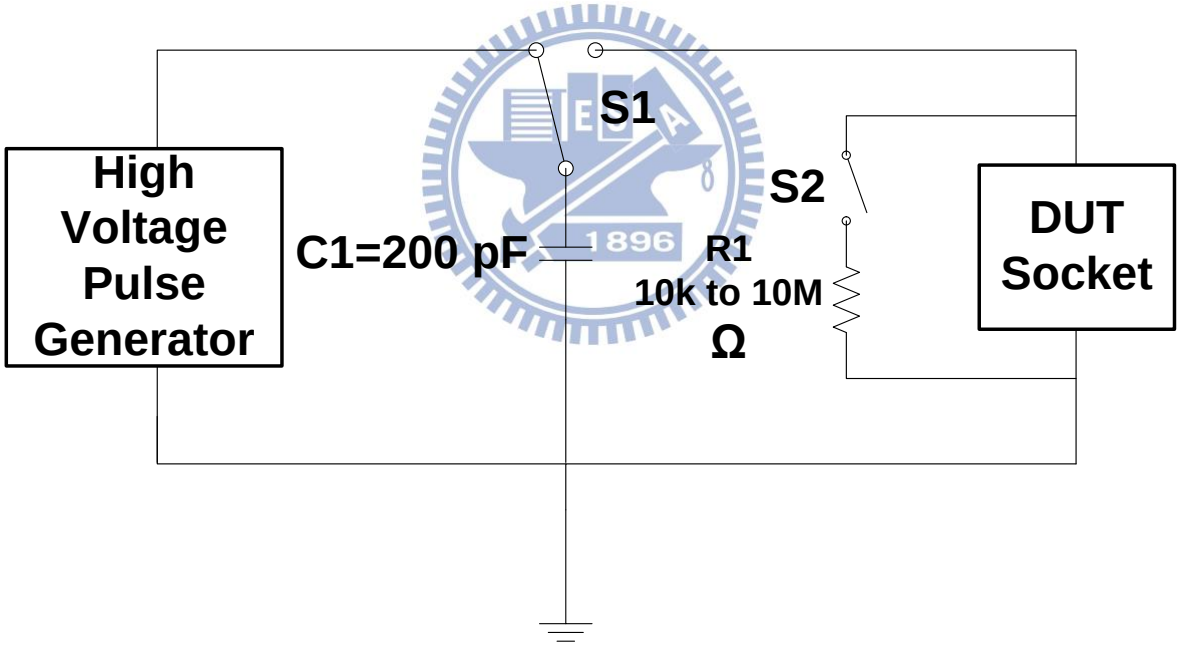


Fig. 4.6 Typical equivalent MM ESD circuit [14].

Therefore, the measurement HBM and MM ESD test zapping level were selected 8 kV and 300 V form TABLE 4.1, respectively. As shown in Fig. 4.7, the measurement setup to verify the current waveform for HBM and MM ESD test. The current prober (CT1) can be measured the peak current change with different stacking numbers. The CT1 provides an output of 5 mV for each milliamp of input current, and the attenuator makes waveform to

decrease by ten times. So the oscilloscope needs to make two times increase to show the real waveform.

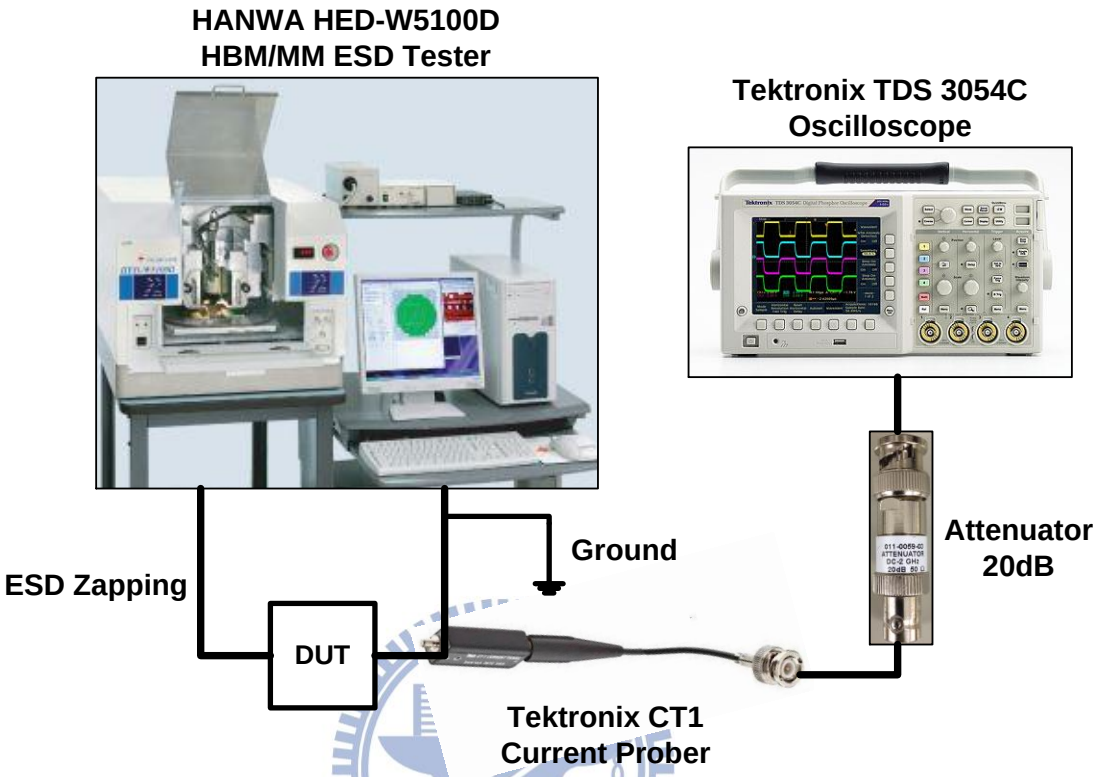


Fig. 4.7 Measurement setup for the HBM and MM ESD current waveform.

4.2.2 Measurement Results

The HBM ESD test is dominated by 1.5 kΩ, and the device resistance is relatively small. Therefore, all the HBM ESD levels are the same. The measurements of HBM current waveform verify the similar level peak currents, rise times, and pulse decay times, as shown in Fig. 4.8. The MM ESD test is dominated by device resistance, because there is no discharge resistance in MM ESD circuit. Therefore, the MM ESD level is proportional to the stacked number of LVPFOD. As shown in Fig. 4.9, the measurements of MM current waveform verify the decreased peak currents, rise times, and first pulse widths by the numbers of stacked LVPFOD. The trend of HBM and MM peak current with different stacking numbers are shown in Fig. 4.10.

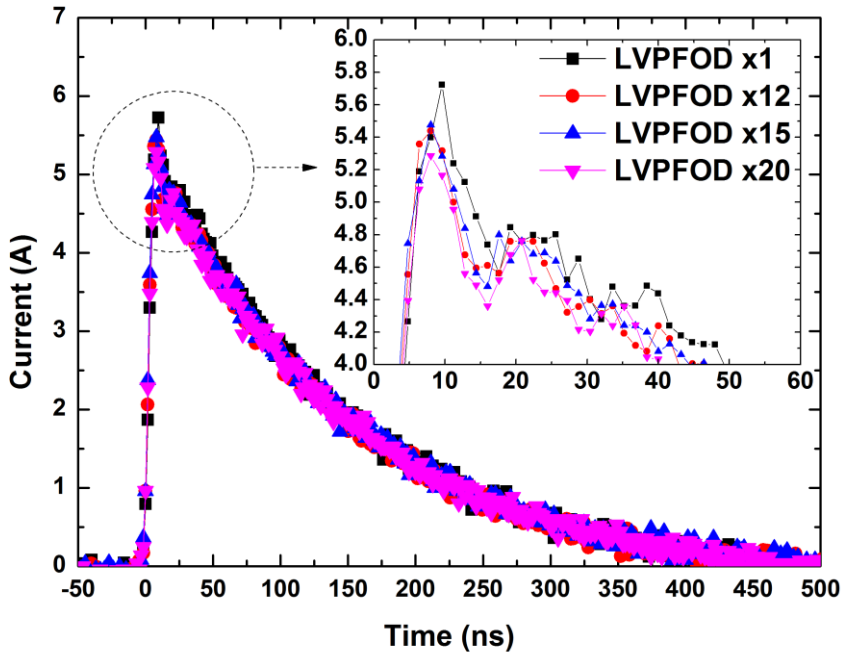


Fig. 4.8 Measured HBM@8kV current waveforms with different stacking numbers of 1, 12, 15, and 20.

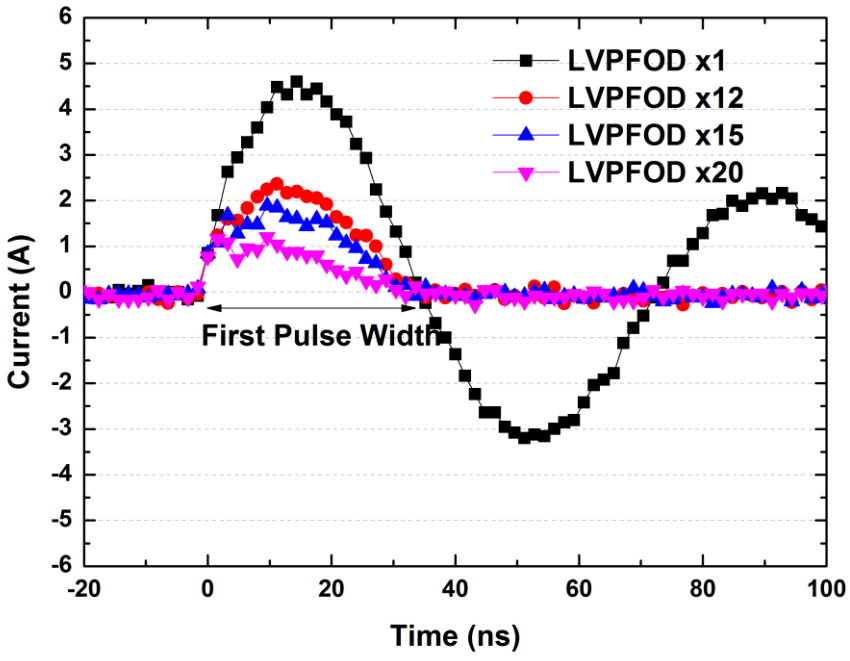


Fig. 4.9 Measured MM@300V current waveforms with different stacking numbers of 1, 12, 15, and 20.

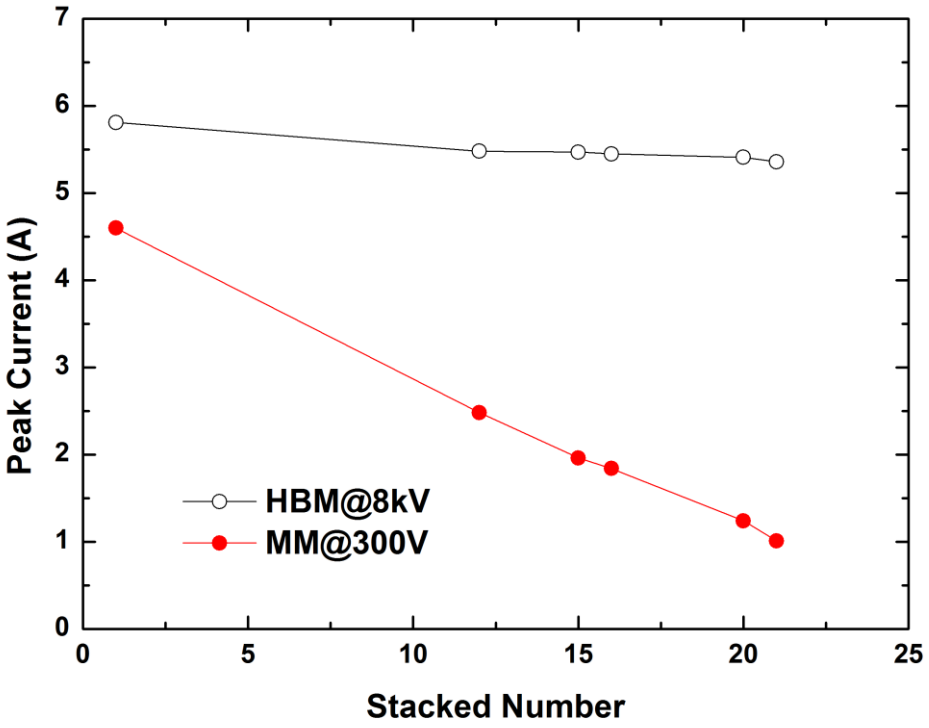


Fig. 4.10 HBM@8kV and MM@300V peak current with different stacking numbers.

The trend of MM rise times and first pulse widths with different stacking numbers are shown in Fig. 4.11. The MM current waveforms measurement verified the decreased rise times and first pulse widths by the numbers of stacked LVPFOD. In condition of the same MM@300 V, by increasing the number of stacked LVPFOD, the peak current is decreased because the device resistance is enlarged. With smaller peak current value, the rise time and the first pulse width would be reduced. Finally, the detailed characteristic of HBM and MM waveforms with different stacking numbers are listed in TABLE 4.2.

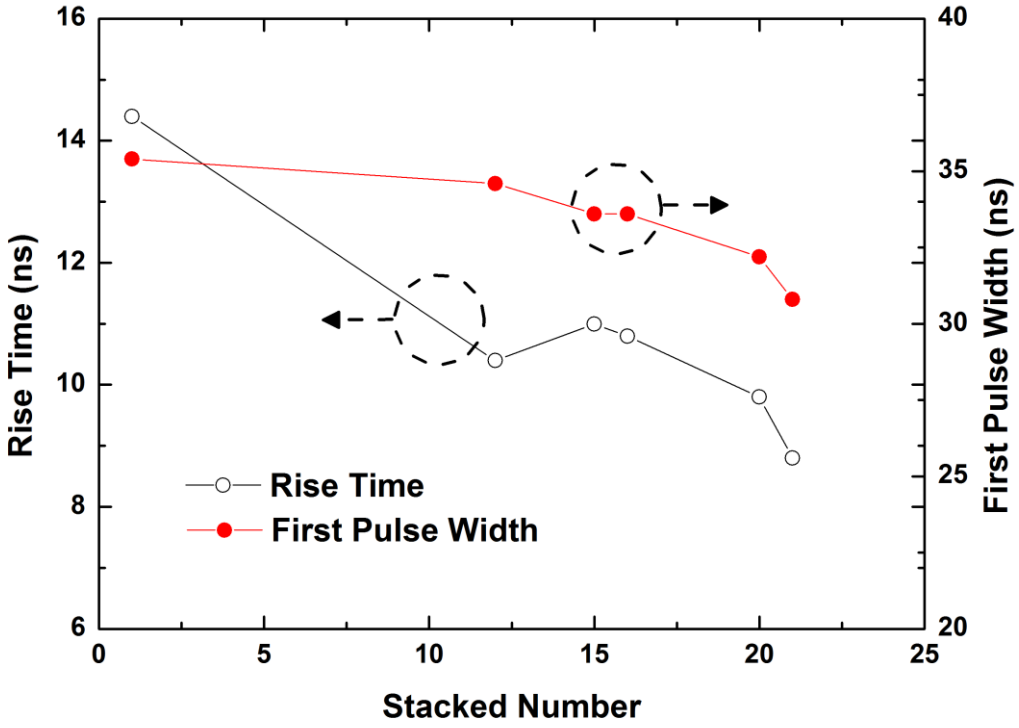


Fig. 4.11 Rise time and first pulse width of MM@300V with different stacking numbers.

TABLE 4.2

Summary of HBM and MM Waveform with Different Stacking Numbers.

Stacked Number of LVPFOD	R_{on} (Ω)	HBM@8 kV			MM@300 V		
		Peak Current (A)	Rise Time (ns)	Pulse Decay Time (ns)	Peak Current (A)	Rise Time (ns)	First Pulse Width (ns)
1	1.39	5.81	9.0	121.2	4.60	14.4	35.4
12	10.77	5.48	7.8	123.6	2.48	10.4	34.6
15	13.11	5.47	8.0	123.6	1.96	11.0	33.6
16	14.63	5.45	6.8	129.6	1.84	10.8	33.6
20	17.17	5.41	8.2	123.6	1.24	9.8	32.2
21	18.13	5.36	7.6	127.0	1.01	8.8	30.8

4.3 Damping Effect

As shown in Fig. 4.9, there are an underdamping and others overdamping in the MM current waveforms. The MM current waveforms are proportional to the stacked number. In this section, there is an investigation of damping effect of MM ESD current waveform. As shown in Fig. 4.12, the differential equation of RLC series circuit can be found the constitutive equation (1) by substituting into Kirchhoff's Voltage Law (KVL), where the source is an unchanging voltage. First of all, differentiating and dividing by inductance (L) leads to the second order differential equation (2). It can usefully be expressed in a more generally applicable form in equation (3). For the case of the series RLC circuit these two parameters are given by α and ω0. And the parameter α, ω0, and ωd are shown in equation (4)-(6). The coefficients C1 and C2 are determined by the boundary conditions of the specific problem being analyzed.

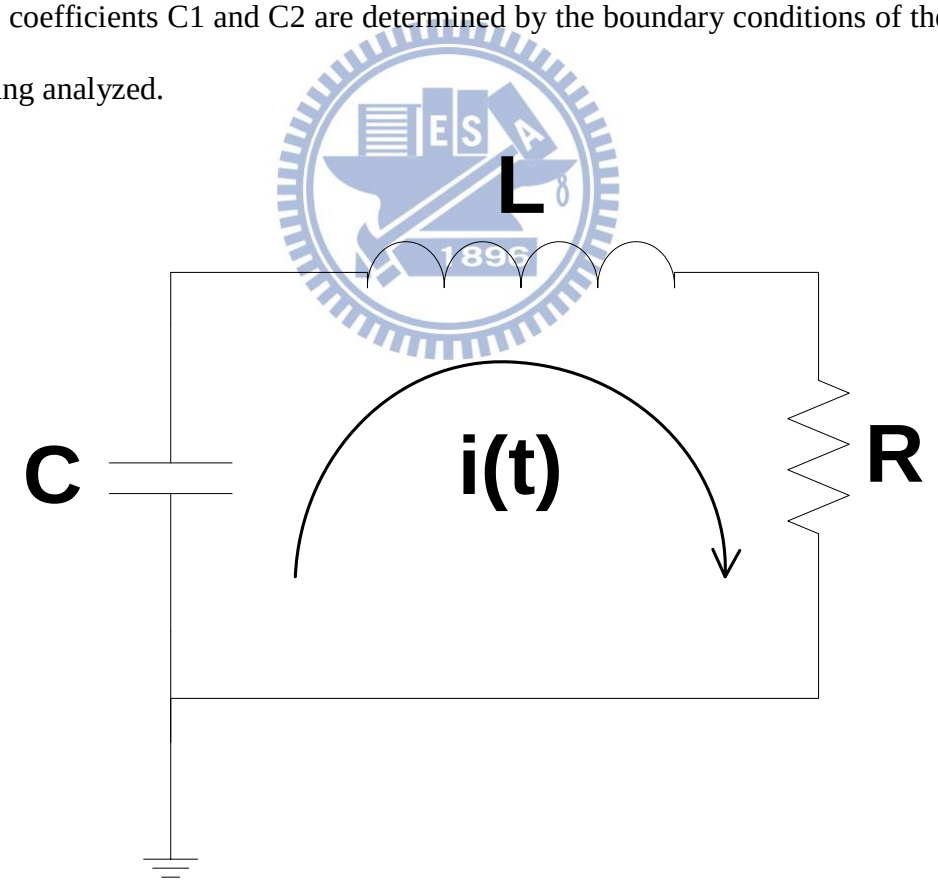


Fig. 4.12 RLC series circuit.

$$Ri(t) + L\frac{di(t)}{dt} + \frac{1}{C}\int_{-\infty}^{\tau=t} i(\tau)d\tau = 0 \quad (1)$$

$$\frac{d^2i(t)}{dt^2} + \frac{R}{L}\frac{di(t)}{dt} + \frac{1}{LC}i(t) = 0 \quad (2)$$

$$\frac{d^2i(t)}{dt^2} + 2\alpha\frac{di(t)}{dt} + {\omega_0}^2 i(t) = 0 \quad (3)$$

$$\alpha = \frac{R}{2L} \quad (4)$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (5)$$

$$\omega_d = \sqrt{{\omega_0}^2 - \alpha^2} \quad (6)$$

$$\xi \triangleq \frac{\alpha}{\omega_0} = \frac{R}{2}\sqrt{\frac{C}{L}} \quad (7)$$

By definition [20], as shown in Fig. 4.13, there are three different current waveforms depending on the value of damping factor (ξ), as shown in equation (7). These are overdamping (ξ > 1), critically damping (ξ = 1), and underdamping (ξ < 1). The differential equation has the characteristic equation as shown in equation (8)-(10). The overdamping waveform is a decay of the transient current without oscillation. The critically damping represents the circuit response that decays in the fastest possible time without going into oscillation. This consideration is important where it is required to reach the desired state as quickly as possible without overshooting. The underdamping waveform is a decaying oscillation at frequency ω_d. The frequency ω_d is shown in equation (6).

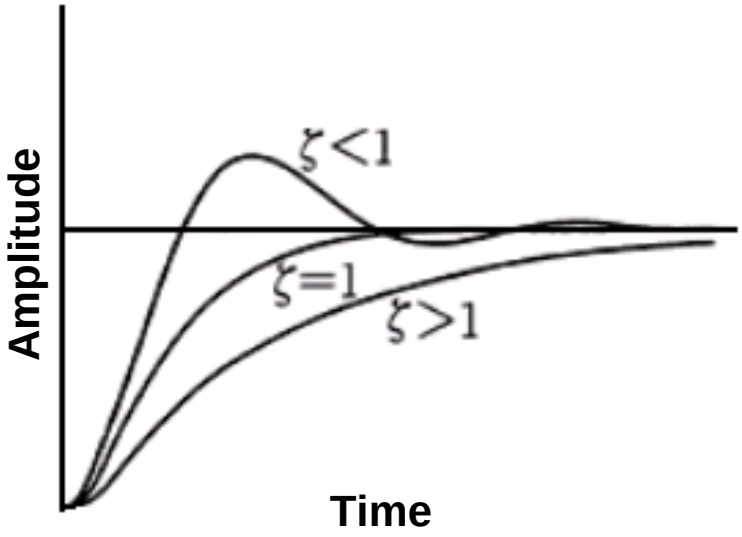


Fig. 4.13 Three different current waveforms.

$$i(t) = \mathrm{A}_1 e^{-\omega_0(\xi+\sqrt{\xi^2-1})t} + \mathrm{A}_2 e^{-\omega_0(\xi-\sqrt{\xi^2-1})t} \tag{8}$$

$$i(t) = \mathrm{B}_1 t e^{-\alpha t} + \mathrm{B}_2 e^{-\alpha t} \tag{9}$$

$$i(t) = \mathrm{C}_1 e^{-\omega_0 t}\cos(\omega_d t) + \mathrm{C}_2 e^{-\omega_0 t}\sin(\omega_d t) \tag{10}$$

As shown in Fig. 4.14, by using the RLC series circuit of MM to explain the measurement result. There are an underdamping and others overdamping in the MM current waveforms, as shown in Fig. 4.9. The MM current waveforms are proportional to the stacked number. The inductance is approximately 0.414 nH for RLC series circuit of MM that is extracted from the measured MM ESD current waveforms. According to the damping factor, when the device resistance is smaller than 2.88 Ω, the MM ESD current waveform will be underdamping. During MM ESD test on a single LVPFOD unit, the current waveform is underdamping. Then the differential equation has the characteristic equation (10) of underdamping waveform. The C and Ron values are 200 pF and 1.39 Ω, respectively. The initial voltage of capacitor is 300 V, and peak current is 4.60 A. As ESD device stacked number increases, the load resistance of MM increases and the peak current decreases. When

the device resistance is larger than 2.88 Ω, the MM ESD current waveform will be overdamping. It is corresponding to the TLP measurement data of R_{on}, as shown in TABLE 4.1.

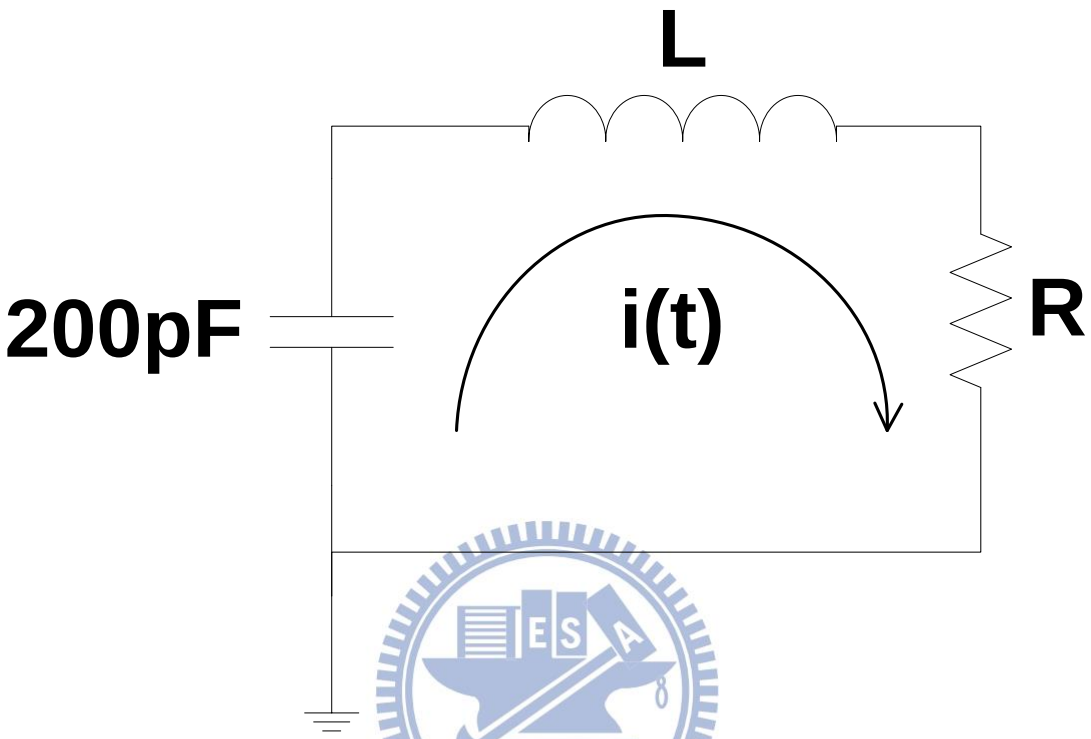


Fig. 4.14 RLC series circuit of MM.

As shown in Fig. 4.8, there are all overdamping in the HBM current waveforms. In the same way as MM, the parameters of HBM RLC series circuit were known. In condition of the unit LVPFOD, the capacitor changes to 100 pF, the Ron is 1.39 Ω, and the resistance adds 1.5 kΩ in series circuit. Also known that the initial voltage of capacitance is 8 kV, and peak current is 5.81 A. Using the same way calculate the overdamping waveform of HBM.

According to the resulting inductance of RLC series circuit of MM is approximately 0.41 nH. As shown in the damping factor in equation (7), if the HBM current waveform is overdamping, the device resistance should be more than 4.07 Ω. The result is much less than 1.5 kΩ. It is easy to know why the definition HBM current waveform in the JEDEC standards is overdamping waveforms.

4.4 Summary

An investigation of HBM and MM effect on stacked ESD protection device for high voltage application is studied in this chapter. This chapter studied the reason why MM ESD level can be increased by the number of stacked ESD devices. As ESD device stacked number increases, the load resistance of MM increases and the peak current decreases. The load resistance of MM is dominated by stacked ESD devices, but the HBM is dominated by 1.5 kΩ. So the MM ESD level increases by the numbers of stacked LVPFOD, and all the HBM ESD level are the same. Damping effect in the equivalent ESD circuit is mainly dominated by the total resistance of ESD discharge path. It determines whether or not the typical equivalent HBM and MM ESD test circuits will resonate naturally.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis, stacked LV devices and stacked LV-HV devices are studied. The characteristic of LVPFOD for ESD protection is better than LVNMOS and LVPMOS. Comparing with stacked HV devices, the stacked LVPFOD has been verified with better ESD robustness in a 0.5-μm SOI process for HV applications. With consideration for layout area and ESD robustness, stacked LVPFOD can be the best choice. The LVPFOD stacked structures can get V_h of 125.55 V, 155.13 V, and 206.49 V for the operation voltages focused on 120 V, 150 V and 200 V, respectively. The silicon data shows that stacked LVPFOD applied for HV application in SOI process can pass 8kV HBM level. By adjusting the stacking numbers, the proposed ESD protection solution can be further used for higher voltage applications and also get latchup-free immunity.

The proposed solution is stacking LV devices for HV ESD protection applications. As ESD device stacked number increases, the load resistance of MM increases and the peak current decreases. Therefore, MM ESD measurement increases by the numbers of stacked devices. The experiment of MM ESD current waveform measurement verified the device resistance increases by the numbers of stacked devices. It has a significant impact on MM ESD level. Also it can explain the waveform damping effect for typical equivalent HBM and MM ESD circuit. Damping effect is caused by the resistance in the circuit. It determines whether or not the typical equivalent HBM and MM ESD test circuits will resonate naturally.

Finally, an effective ESD protection solution realized with stacked LVPFOD has been successfully verified in a VIS 0.5-μm SOI process for HV applications. Stacked LV devices not only get higher ESD robustness, but also use fewer layout layers. The experiment of MM

ESD current waveform measurement verified the MM ESD level is proportional to the stacked number.

5.2 Future Work

In this thesis, there is a solution with high ESD robustness and latchup-free immunity. It can meet ESD protection design window. But layout area of the stacked devices for ESD protection is still large. By modifying the layer of LV device structure, the breakdown voltage can be increased. It is possible to decrease the stacked number of LV devices for circuit operation voltage. It can reduce a relatively small layout area.

There is a HV application for bidirectional HV ESD protection. The bidirectional HV ESD protection with latchup-free immunity design is requested in some HV applications with input voltage maybe lower than Vss. A bidirectional device provides ESD protection for both polarities in a single device. Using the method of stacked LV devices, it would waste more area for HV ESD protection. To investigate the methods for bidirectional HV ESD protection with latchup-free immunity design is the next research.

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Publication List

[1] Yi-Jie Huang, Ming-Dou Ker, Yeh-Jen Huang, Chun-Chien Tsai, Yeh-Ning Jou, and Geeng-Lih Lin, “ESD Protection Design with Latchup-Free Immunity in 120V SOI Process,” accepted by *IEEE International Conference SOI-3D-Subthreshold Microelectronics Technology Unified*.

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